Errata

Title & Document Type: excerpt from:
44711A/12A/13A High Speed Multiplexer Service Guide

Manual Part Number: 44711-99000

Revision Date: September 1, 1986

HP References in this Manual

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CHAPTER 10
HP 44711A/44712A/44713A
HIGH SPEED FET MULTIPLEXER

CHAPTER 10
HP 44711A/44712A/44713A
HIGH-SPEED FET MULTIPLEXERS

10-1 INTRODUCTION

This chapter provides a technical description, performance test procedures, and replaceable parts lists for the HP 44711A 24 Channel High-Speed FET Multiplexer, HP 47712A 48 Channel Single Ended High-Speed FET Multiplexer, and HP 44713A 24 Channel High-Speed FET Multiplexer with Thermocouple Compensation. All three FET multiplexers use the same component module and are made unique by the addition of the terminal modules.

10-2 HP 44711A Technical Description

The HP 44711A 24 Channel High-Speed FET Multiplexer has two main assemblies: the component module and the terminal module. The component module contains the backplane interface electronics, the ribbon cable interface electronics, the switching FETs, the FET control logic, and the isolation relay control logic. The terminal module contains terminal strips for connection to external wiring and provides mounting holes for user installed parts such as one pole low pass filters or voltage dividers. The printed circuit board used in the component module is also used in the HP 44712A and HP 44713A component modules.

Figure 10-1 shows a simplified schematic of the HP 44711A. In the component module the FET switches are arranged into channel switches and tree switches. There are 48 channel switches arranged and switched in pairs. Each channel switch pair switches a high line and a low line. The channel switches are arranged into two banks, referred to as Bank A and Bank B. There are 12 channels in each bank and each bank has its own set of common terminals. Only one channel in each bank can be closed at the same time.

The tree switches allow the multiplexer channels to be connected to either the backplane analog bus or the high-speed voltmeter ribbon cable. There are eight tree switches arranged and switched in pairs. Each tree switch pair switches a high line and a low line. Two of the tree switch pairs connect to the sense bus and two connect to the source bus. The sense bus is used for measurements. The source bus provides a current source for resistance measurements. The current on the source bus is provided by either an HP 44701A through the backplane analog bus or an HP 44702A/B through either the backplane analog bus or the ribbon cable.

The tree switches are controlled independently of the channel switches in the high level commands. The tree switches are controlled by the use of channel numbers 91, 92, 93, and 94. Channel 91 controls the source bus tree switch, channel 92 controls the sense bus tree switch, channel 93 configures the HP 44711A for two-wire ohms measurements, and channel 94 configures the HP 44711A for four-wire ohms measurements.

The HP 44711A is specifically designed to connect to an HP 44702A/B High-Speed Voltmeter. The ribbon cable is provided for this purpose. The HP 44702A/B is able to control the multiplexer switches and take measurements through the ribbon cable. This control can be established independently of the HP 3852A backplane. The connection of one or more high-speed FET multiplexers with the HP 44702A/B through the ribbon cable creates a separate subsystem within the HP 3852A system.

Isolation relays are provided on the HP 44711A. These relays allow the FET multiplexer to be completely isolated from the backplane analog bus. The state of these relays are controlled by assigning them channel

number 90. Once the isolation relays have been closed, they will remain closed until specifically instructed to open or a reset occurs. The isolation relays can be opened to reduce the leakage current on the backplane analog bus for critical measurements. Also, since the backplane analog sense bus can have up to 42 V peak (with an HP 44711A installed), the isolation relays provide protection for the FET switches. If, for example, an application requires that the backplane analog sense bus voltage is greater than 12 V peak, the isolation relays should be opened to prevent damage to the FET switches. In addition, the FETs are protected from voltages above 16 Vdc by the overvoltage protection circuit on the multiplexer assembly (the input impedance to the FETs, however, decreases above 12 V peak). The overvoltage protection circuit automatically opens the isolation relays, if the backplane analog bus voltage exceeds 16 Vdc.

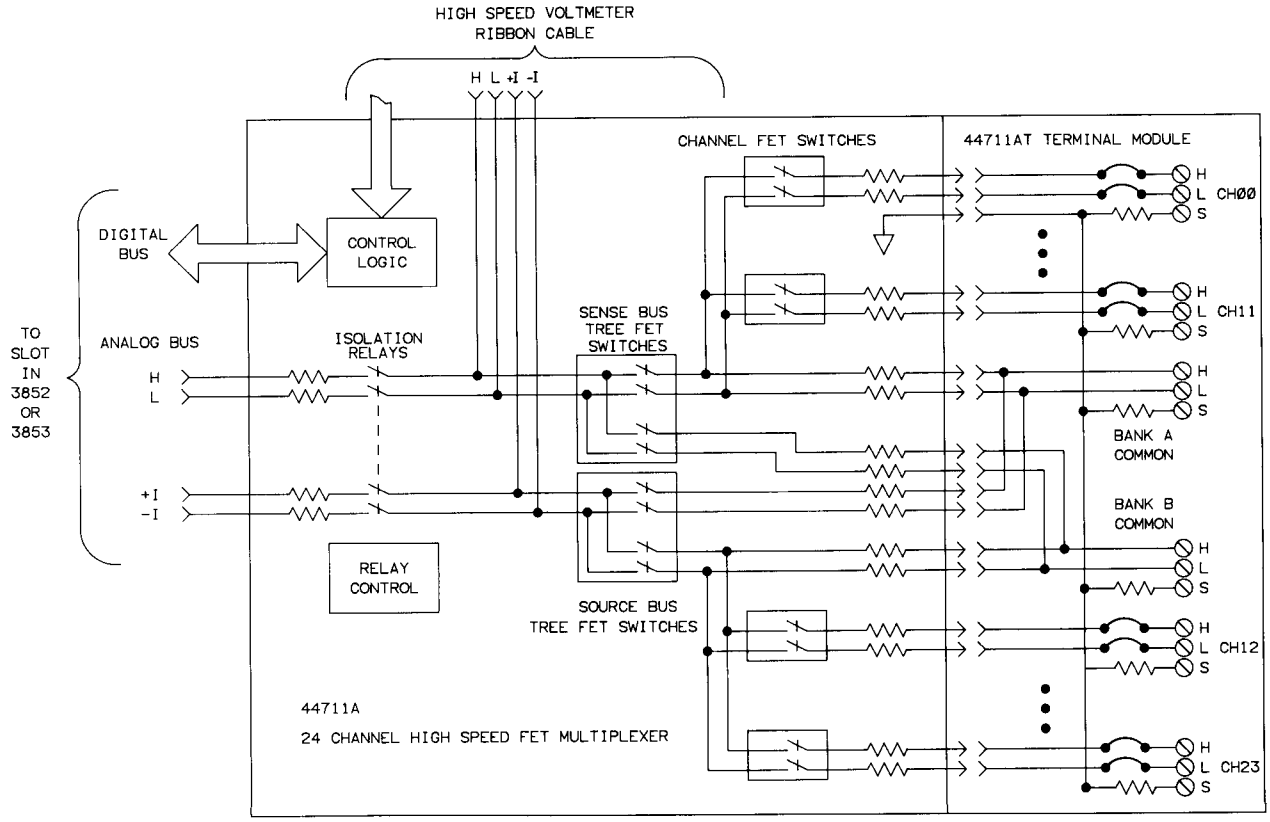


Figure 10-1 HP 44711A Simplified Schematic

10-3 HP 44712A Technical Description

The HP 44712A 48 Channel Single Ended High-Speed FET Multiplexer has two main assemblies: a component module and a terminal module. The component module contains the backplane interface electronics, the ribbon cable interface electronics, the FET control logic, and the isolation relay control logic. The terminal module contains terminal strips for connection to external wiring. The printed circuit board used in the component module is also used in the HP 44711A and HP 44713A component modules. The terminal module is unique.

Figure 10-2 shows a simplified schematic of the HP 44712A. In the component module the FET switches are arranged into channel switches and tree switches. There are 48 channel switches arranged and switched in pairs. Each channel switch pair switches two channel high lines into the tree switches. The low lines for all channels are common on the terminal module and are connected to the component module circuit ground through a 100 ohm resistor.

The tree switches connect the multiplexer channels to either the backplane analog bus or the high-speed voltmeter ribbon cable. There are eight tree switches arranged and switched in pairs. Each tree switch pair switches a channel high line and circuit ground. The tree switches allow selection of a single channel from the paired channel switches. Two of the tree switch pairs are connected to the sense bus and two are connected to the source bus. The sense bus is used for measurements. The source bus provides a current source for resistance measurements. The current on the source bus is provided by either an HP 44701A through the backplane analog bus or by an HP 44702A/B through either the backplane analog bus or the ribbon cable.

The tree switches are controlled independently of the channel switches in the high level commands. The tree switches are controlled by use of channel numbers 91, 92, and 93. Channel 91 connects the source bus, channel 92 connects the sense bus, and channel 93 configures the HP 44712A for two-wire ohms measurements.

The HP 44712A is specifically designed to connect to an HP 44702A/B High-Speed Voltmeter. The ribbon cable is provided for this purpose. The HP 44702A/B is able to control the multiplexer switches and take measurements through the ribbon cable. This control can be established independently of the HP 3852A backplane. The connection of one or more high-speed FET multiplexers with the HP 44702A/B through the ribbon cable creates a separate subsystem within the HP 3852A system.

Isolation relays are provided on the HP 44712A. These relays allow the FET multiplexer to be completely isolated from the backplane analog bus. The state of these relays are controlled by assigning them channel number 90. Once the isolation relays have been closed, they will remain closed until specifically instructed to open or a reset occurs. The isolation relays can be opened to reduce the leakage current on the backplane analog bus for critical measurements. Also, since the backplane analog sense bus can have up to 42 V peak (with an HP 44712A installed), the isolation relays provide protection for the FET switches. If, for example, an application requires that the backplane analog sense bus voltage is greater than 12 V peak, the isolation relays should be opened to prevent damage to the FET switches. In addition, the FETs are protected from voltages above 16 Vdc by the overvoltage protection circuit on the multiplexer assembly (the input impedance to the FETs, however, decreases above 12 V peak). The overvoltage protection circuit automatically opens the isolation relays, if the backplane analog bus voltage exceeds 16 Vdc.

10-4 HP 44713A Technical Description

The HP 44713A has two main assemblies: a component module and a terminal module. The component module contains the backplane interface electronics, the ribbon cable interface electronics, the FET control logic and the isolation relays control logic. The terminal module contains terminal strips for connection to external wiring, a thermistor in an isothermal block, and provides mounting holes for user installed parts such as one pole low pass filters or voltage dividers. The printed circuit board used in the component module is also used the HP 44711A and HP 44712A component modules. The terminal module is unique.

Figure 10-3 shows a simplified schematic of the HP 44713A. In the component module the FET switches are arranged into channel switches and tree switches. There are 48 channel switches arranged and switched in pairs. Each channel switch pair switches a high line and a low line. One set of multiplexer common terminals is provided on the terminal module.

The tree switches allow the multiplexer channels to be connected to either the backplane analog bus or the high-speed voltmeter ribbon cable. There are eight tree switches arranged and switched in pairs. Each tree switch pair switches a high line and a low line. Two of the tree switch pairs connect to the sense bus and two connect to the source bus. The sense bus is used for measurements. The source bus provides a current source for resistance measurements. The current on the source bus is provided by either an HP 44701A through the backplane analog bus or an HP 44702A/B through either the backplane analog bus or the ribbon cable.

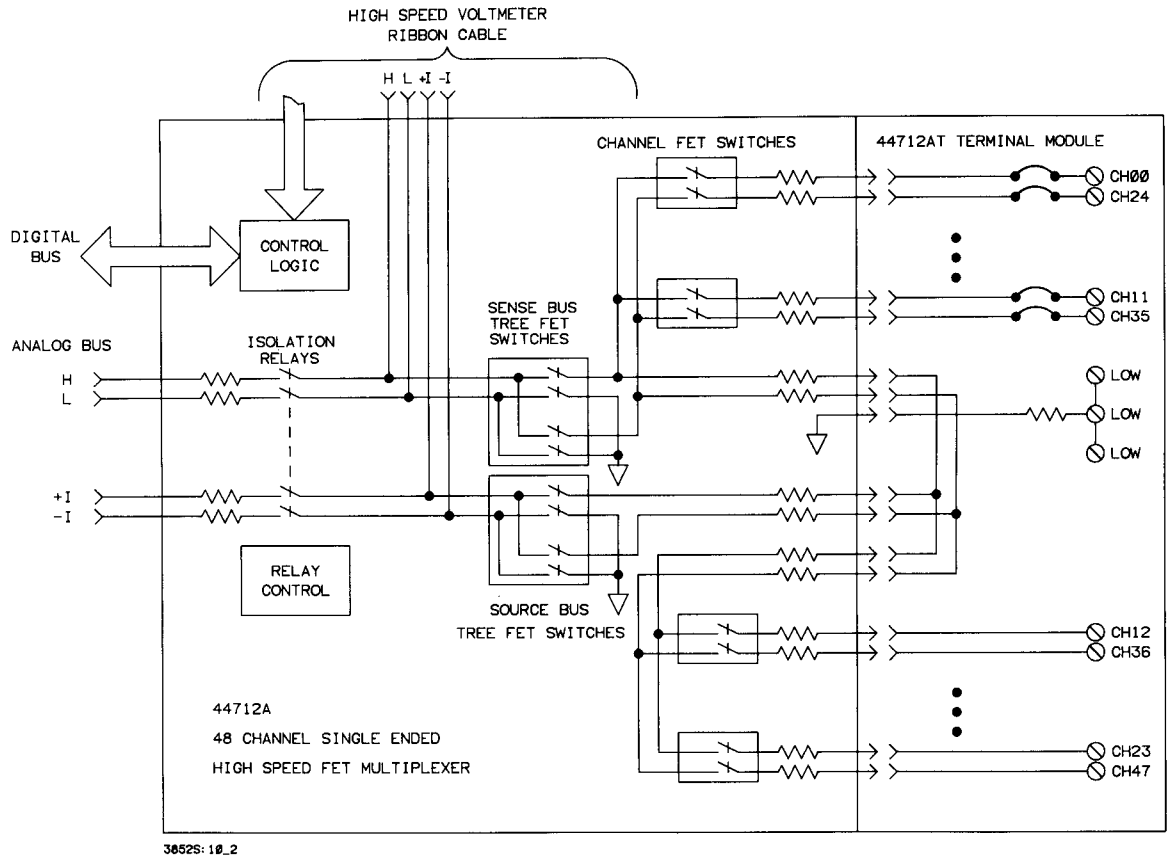


Figure 10-2 HP 44712A Simplified Schematic

The tree switches are controlled independently of the channel switches in the high level commands. The tree switches are controlled by the use of channel numbers 91, 92, 93, and 94. Channel 91 controls the source bus tree switch, channel 92 controls the sense bus tree switch, channel 93 configures the HP 44713A for two-wire ohms measurements and channel 94 configures the HP 44713A to measure the thermistor.

The HP 44713A is specifically designed to connect to an HP 44702A/B High-Speed Voltmeter. The ribbon cable is provided for this purpose. The HP 44702A/B is able to control the multiplexer switches and take measurements through the ribbon cable. This control can be established independently of the HP 3852A backplane. The connection of one or more high-speed FET multiplexers with the HP 44702A/B through the ribbon cable creates a separate subsystem within the HP 3852A system.

Isolation relays are provided on the HP 44713A. These relays allow the FET multiplexer to be completely isolated from the backplane analog bus. The state of these relays are controlled by assigning them channel number 90. Once the isolation relays have been closed, they will remain closed until specifically instructed to open or a reset occurs. The isolation relays can be opened to reduce the leakage current on the backplane analog bus for critical measurements. Also, since the backplane analog sense bus can have up to 42 V peak (with an HP 44713A installed), the isolation relays provide protection for the FET switches. If, for example, an application requires that the backplane analog sense bus voltage is greater than 12 V peak, the isolation relays should be opened to prevent damage to the FET switches. In addition, the FETs are protected from voltages above 16 Vdc by the overvoltage protection circuit on the multiplexer assembly (the input impedance to the FETs, however, decreases above 12 V peak). The overvoltage protection circuit automatically opens the isolation relays, if the backplane analog bus voltage exceeds 16 Vdc.

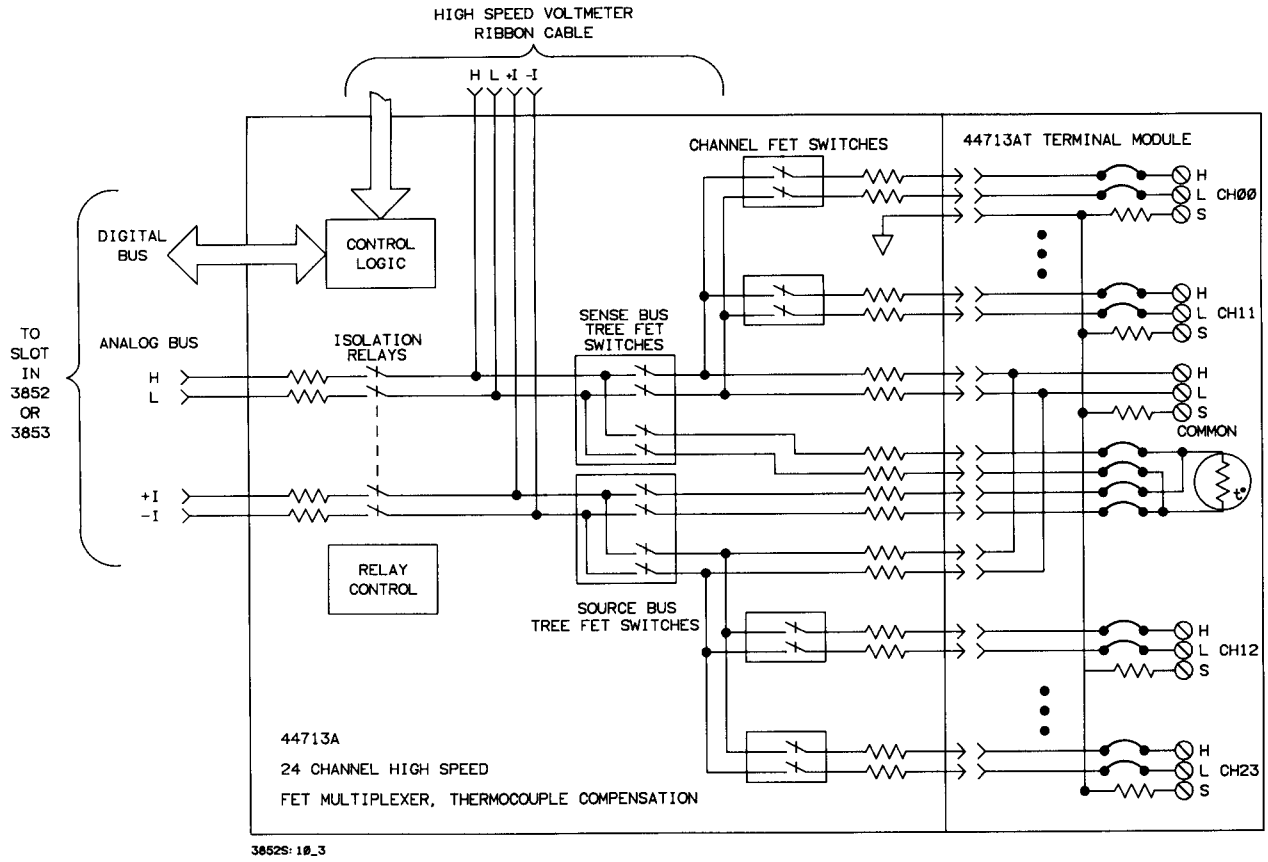


Figure 10-3 HP 44713A Simplified Schematic

10-5 Read and Write Registers

The HP 3852A communicates with each plug-in accessory by using read and write registers. High level commands are translated into appropriate register commands. The SREAD and SWRITE commands can be used to directly control each register.

SREAD and SWRITE are described in Chapter 2 of this manual. Table 10-1 shows the registers used by the HP 44711A, HP 44712A, and HP 44713A.

CAUTION

Using the primitive commands (SREAD and SWRITE) may cause unexpected and undesirable effects on the plug-in accessories. It is possible to program some plug-in accessories into illegal and potentially damaging states with these commands. The commands are documented here for service purposes only.

10-6 Read Registers

NOTE

The decimal number returned after the execution of an SREAD command represents the two's compliment of the status word.

Table 10-1 High-Speed FET Multiplexer Read and Write Registers

Register #	READ Registers	WRITE Registers
0	Accessory Identification	Accessory Reset
1	Accessory Status	Accessory Address
2	FET Switch Status	Not used
3	Not Used	FET Opening
4	Not Used	Isolation Relays Opening
5	Not Used	Isolation Relays Closing
6	Not used	FET Closing
7	Not Used	Not Used

10-7 Register 0. Read Register 0 contains the accessory identification. Eight bits are used to uniquely identify the accessory. The eight bits are output on the lower eight bits of the backplane data bus.

The eight bit identification is in two parts. The five most significant bits identify the component module installed. The least significant three bits identify the type of terminal module installed. If the terminal module is not present, the lower three bits are set high by the component module. If a terminal module is installed, the type of terminal module is also identified.

Table 10-2 lists the decimal equivalent codes returned in response to an SREAD of Register 0 for all combinations of the modules. Note that all three FET multiplexers use the same component module, identified as an HP 44711A in Table 10-2.

Table 10-2 HP 44711A, HP 44712A, and HP 44713A Identification Codes

Module Combinations	Codes
HP 44711A Component Module (no terminal module installed)	-137
HP 44711A Component Module, HP 44711AT Terminal Module installed	-141
HP 44711A Component Module, HP 44712AT Terminal Module installed	-139
HP 44711A Component Module, HP 44713AT Terminal Module installed	-144

10-8 Register 1. Read Register 1 is the accessory status register. This register uses backplane data bits 0 through 7 to indicate the current operating status of the accessory to the HP 3852A local controller. The following paragraphs describe the meaning of each bit in the status word.

Bit 7 indicates the status of the isolation relays. Bit 7 is set high when the isolation relays have been instructed to open and low when instructed to close. It is possible that the status bit will not correctly indicate the status of the isolation relays if the register is read too soon after the close or open command has

been sent. The period of uncertainty is 1 millisecond after a close command and 0.5 millisecond after an open command.

Bit 6 is used to indicate the connection status of the ribbon cable. When the ribbon cable is connected to an HP 44702A/B bit 6 is pulled low.

Bit 5 is used to indicate the active bus for switch control. A high level indicates that the accessory control has been assigned to the HP 44702A/B High-Speed Voltmeter. A low level indicates that the accessory control is assigned to the HP 3852A backplane bus.

Bit 4 is set low when a HP 44702A/B High-Speed Voltmeter scan is in progress. The bit returns high when the scan is completed. A scan operation also sets bit 1 high so bits 4 and 1 can be used to determine if the accessory is currently scanning or is busy processing a command.

Bit 3 indicates the current status of the HP 3852A backplane OPENING line. When the OPENING pulse on the backplane is asserted, bit 3 is set high.

Bit 2 is the local opening signal. Bit 2 is set high while the multiplexer is opening a switch.

Bit 1 indicates the busy/ready status of the multiplexer. When bit 1 is set high the multiplexer is processing the last command or is involved in a scan operation. When bit 1 is high no write operations should be made to the multiplexer. Bit 1 is set low to indicate that the multiplexer is ready to accept a new command.

Bit 0 is fixed low.

10-9 Register 2. Read Register 2 is the switch status register. Figure 10-4 shows the eight bits returned from the switch status register.

7	6	5	4	3	2	1	0
0	0	0	0	C	C	C	C

Figure 10-4 Read Register 2

The most significant four bits, D4 through D7, are an operation code that provides an indication of the tree switch states and the channel bank that is currently enabled. Bits D0 through D3 provides an indication of the channel number that is being used with the operation codes. Table 10-3 gives the operation codes for the HP 44711A. Table 10-4 gives the operation codes for the HP 44712A and Table 10-5 gives the operation codes for the HP 44713A. The channel number codes for the HP 44711A and HP 44713A are given in Table 10-6. Channel codes for the HP 44712A are given in Table 10-7.

10-10 Write Registers

10-11 Register 0. Write Register 0 is the accessory reset register. Any data written to this register will open any FET switches closed, open the isolation relays, and stop opening and closing coordination on the backplane. A write to register 0 produces the same results as a system reset (backplane reset).

10-12 Register 1. Write Register 1 is the accessory address register. The address register is used to assign each FET multiplexer a unique address on the ribbon cable. The address is used when the FET Multiplexers are being controlled by the HP 44702A/B over the ribbon cable. Additionally the address register uses one bit to set the control of the FET multiplexer to either the HP 3852A backplane or the HP 44702A/B. Figure 10-5 shows the accessory address word.

Table 10-3 HP 44711A Operation Codes

Code	Tree Switches	Bank Enabled
0000	None	Bank B
0001	None	Bank B
0010	None	Bank A
0011	None	Bank A
0100	Bank A source bus	Bank B
0101	Bank B source bus	Bank B
0110	Bank A source bus	Bank A
0111	Bank B source bus	Bank A
1000	Bank A sense bus	Bank B
1001	Bank B sense bus	Bank B
1010	Bank A sense bus	Bank A
1011	Bank B sense bus	Bank A
1100	Bank A sense, Bank B source	Bank A, Bank B
1101	Bank B sense, Bank B source	Bank B
1110	Bank A sense, Bank A source	Bank A
1111	Bank B sense, Bank A source	Bank A, Bank B

Table 10-4 HP 44712A Operation Codes

Code	Tree Switches	Channels Enabled
0000	None	12-23, 36-47
0001	None	12-23, 36-47
0010	None	00-11, 24-35
0011	None	00-11, 24-35
0100	Ch 24-47 source bus	12-23, 36-47
0101	Ch 0-23 source bus	12-23, 36-47
0110	Ch 24-47 source bus	00-11, 24-35
0111	Ch 0-23 source bus	00-11, 24-35
1000	Ch 24-47 sense bus	12-23, 36-47
1001	Ch 0-23 sense bus	12-23, 36-47
1010	Ch 24-47 sense bus	00-11, 24-35
1011	Ch 0-23 sense bus	00-11, 24-35
1100	Ch 24-47 sense and source	12-23, 36-47
1101	Ch 0-23 sense and source	12-23, 36-47
1110	Ch 24-47 sense and source	00-11, 24-35
1111	Ch 0-23 sense and source	00-11, 24-35

Table 10-5 HP 44713A Operation Codes

Code	Tree Switches	Channels Enabled
0000	None	Ch 12-23
0001	None	Ch 12-23
0010	None	Ch 00-11
0011	None	Ch 00-11
0100	Source to common	Ch 12-23
0101	Source to thermistor	Ch 12-23
0110	Source to common	Ch 00-11
0111	Source to thermistor	Ch 00-11
1000	Sense to common	Ch 12-23
1001	Sense to thermistor	Ch 12-23
1010	Sense to common	Ch 00-11
1011	Sense to thermistor	Ch 00-11
1100	Sense and source to common	Ch 12-23
1101	Sense and source to thermistor	Ch 12-23
1110	Sense and source to common	Ch 00-11
1111	Sense and source to thermistor	Ch 00-11

Table 10-6 HP 44711A and HP 44713A Channel Codes

Code	Channel	Code	Channel
0000	None	1000	7 (19)
0001	None	1001	6 (18)
0010	None	1010	5 (17)
0011	None	1011	4 (16)
0100	11 (23)	1100	3 (15)
0101	10 (22)	1101	2 (14)
0110	9 (21)	1110	1 (13)
0111	8 (20)	1111	0 (12)

Table 10-7 HP 44712A Channel Codes

Code	Channel	Code	Channel
0000	None	1000	7 & 31 (19 & 43)
0001	None	1001	6 & 30 (18 & 42)
0010	None	1010	5 & 29 (17 & 41)
0011	None	1011	4 & 28 (16 & 40)
0100	11 & 35 (23 & 47)	1100	3 & 27 (15 & 39)
0101	10 & 34 (22 & 46)	1101	2 & 26 (14 & 38)
0110	9 & 33 (21 & 45)	1110	1 & 25 (13 & 37)
0111	8 & 32 (20 & 44)	1111	0 & 24 (12 & 36)

7	6	5	4	3	2	1	0
X	X	X	X	B	A	A	A

Figure 10-5 Write Register 1 Accessory Address Word

In the accessory address word, bits 4 through 7 are not used. Bit 3 is the bus control bit. When this bit is set high, the control of the FET Multiplexer is given to the HP 44702A/B. When set low, control returns to the HP 3852A backplane. Bits 0 through 2 are the address bits. Typically, the addresses assigned correspond to the slot number where the FET Multiplexer is installed.

10-13 Register 3. Write Register 3 is the Opening register. A write to this register opens the FET switches indicated in the command word. The command word is described in Section 10-17. When the command word is sent to register 3, the backplane OPENING line is pulsed to coordinate the break-before-make feature.

10-14 Register 4. Write Register 4 opens the isolation relays. Any data sent to this register causes the isolation relays to open and pulses the HP 3852A backplane OPENING line.

10-15 Register 5. Write Register 5 closes the isolation relays. Any data written to this register initiates the closing of the isolation relays. Before the relay closes, the HP 3852A backplane OPENING line is examined. If the OPENING line is low the relays closure is delayed until the line returns high. When the isolation relays are closing the HP 3852A backplane CLOSING line is pulsed.

10-16 Register 6. Write Register 6 is the is the FET switch closing register. A write to this register will close the FET switches indicated in the command word. The command word is described in Section 10-17. When the command word is sent to this register the HP 3852A backplane CLOSING line is pulsed.

10-17 Command Word

The command word uses 15 bits. The bits are arranged into isolation relays control, tree switch operation code bits, and channel bits. The command word is shown in Figure 10-6. The command word is used for both opening and closing functions. The function is determined by the register receiving the command word.

Bits:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Use:	C	X	X	X	X	X	X	X	0	0	0	0	C	C	C	C

Figure 10-6 Command Word

Bit 15 controls the isolation relays. Bits 8 through 14 are not used and will be ignored. Bits 4 through 7 are the tree switch operation codes bits. The operation codes for the FET Multiplexers are shown in Tables 10-3, 10-4 and 10-5. Bits 0 through 3 are the channel control bits. The actual channels that these bits control is determined by the operation code in bits 4 through 7. The channel codes for the FET multiplexers are given in Tables 10-6 and 10-7. The decimal number sent by an SWRITE command represents the two's compliment of the command word.

10-18 SPECIFICATIONS

Specifications for the HP 44711A, HP 44712A and HP 44713A are given in Table 10-8. Specifications are the performance standards or limits against which the FET multiplexers may be tested.

CAUTION

The installation of the HP 44711A, HP 44712A, or HP 44713A reduces the maximum allowable backplane voltages to 42 V peak.

Table 10-8 HP 44711A/44712A/44713A Specifications

HP 44711A 24 Channel High Speed FET Multiplexer

Maximum Switch Rates: 5500 channels/second (from back-plane)*
100000 channels/second (from ribbon cable)

Maximum Input Voltage: Rear and back-plane inputs protected to 16 V peak (input impedance decreases above 12 V due to internal protection circuitry). With analog back-plane disconnected from multiplexer, the back-plane voltage can go up to 42 V peak.

Maximum Input Current: 1 mA non-inductive per channel

Input Impedance:

Impedance	Terminals	
	High to Low	High or Low to Chassis
Power On Resistance (Ω)	$>10^8$	$>10^8$
Power Off Resistance (Ω) Vin 10 V	>1000	>1000
Power Off Resistance (Ω) Vin >10 V	>200	>200
Max. Capacitance (pf) at 1MHz	200	200

Closed Channel Path Resistance: 3.1 kΩ for either High or Low Inputs considered separately

Bandwidth: 1.0% flatness at 20 kHz, -3 dB Bandwidth at 200 kHz (50 Ω source, 1 MΩ termination)

Crosstalk: -50 dB at 10 kHz, -35 dB at 100 kHz (channel-to-channel, 50 Ω source, 1 MΩ termination)

Maximum Offset Voltage: 15 µV at 0 to 28 °C
185 µV at 28 to 55 °C
(offset voltage between High and Low)

Maximum Bias Current: ±5 nA DC at 0 to 28 °C
±15 nA DC at 28 to 55 °C
(Current sourced by High or Low to Chassis into Input Terminals or back-plane, with isolation relays closed)

±1 nA DC at 0 to 55 °C
(Current sourced by High or Low to Chassis into back-plane, with isolation relays open)

Maximum Wire Size: 16 AWG

Table 10-8 HP 44711A/44712A/44713A Specifications (Cont.)

HP 44712A 48 Channel Single Ended High Speed FET Multiplexer

Maximum Switch Rates: 5500 channels/second (from back-plane)*
100000 channels/second (from ribbon cable)

Maximum Input Voltage: Rear and back-plane inputs protected to 16 V peak (input impedance decreases above 12 V due to internal protection circuitry). With analog back-plane disconnected from multiplexer, the back-plane voltage can go up to 42 V peak.

Maximum Input Current: 1 mA non-inductive per channel

Input Impedance: High to Low, $>10^8$ Ω, <=200 pF (at 1 MHz)
Power Off Resistance, >1000 Ω (Vin <=10 V)
Power Off Resistance, >200 Ω (Vin >10 V)

Closed Channel Path Resistance: 3.1 kΩ for either High or Low Inputs considered separately

Bandwidth: 1.0% flatness at 20 kHz, -3 dB Bandwidth at 200 kHz (50 Ω source, 1 MΩ termination)

Crosstalk: -50 dB at 10 kHz, -35 dB at 100 kHz (channel-to-channel, 50 Ω source, 1 MΩ termination)

Maximum Offset Voltage: 15 µV at 0 to 28 °C
185 µV at 28 to 55 °C
(offset voltage between High and Low)

Maximum Bias Current: ±5 nA DC at 0 to 28 °C
±15 nA DC at 28 to 55 °C
(Current sourced by High or Low to Chassis into Input Terminals or back-plane, with isolation relays closed)

±1 nA DC at 0 to 55 °C
(Current sourced by High or Low to Chassis into back-plane, with isolation relays open)

Maximum Wire Size: 16 AWG

HP 44713A 24 Channel High Speed FET Mux with Thermocouple Compensation

Maximum Switch Rates: 5500 channels/second (from back-plane)*
100000 channels/second (from ribbon cable)

Table 10-8 HP 44711A/44712A/44713A Specifications (Cont.)

Maximum Input Voltage: Rear and back-plane inputs protected to 16 V peak (input impedance decreases above 12 V due to internal protection circuitry). With analog back-plane disconnected from multiplexer, the back-plane voltage can go up to 42 V peak.

Maximum Input Current: 1 mA non-inductive per channel

Input Impedance:

Impedance	Terminals	
	High to Low	High or Low to Chassis
Power On Resistance (Ω)	$>10^8$	$>10^8$
Power Off Resistance (Ω) Vin 10 V	>1000	>1000
Power Off Resistance (Ω) Vin >10 V	>200	>200
Max. Capacitance (pf) at 1MHz	200	200

Closed Channel Path Resistance: 3.1 kΩ for either High or Low Inputs considered separately

Bandwidth: 1.0% flatness at 20 kHz, -3 dB Bandwidth at 200 kHz (50 Ω source, 1 MΩ termination)

Crosstalk: -50 dB at 10 kHz, -35 dB at 100 kHz (channel-to-channel, 50 Ω source, 1 MΩ termination)

Maximum Offset Voltage: 15 µV at 0 to 28 °C
185 µV at 28 to 55 °C
(offset voltage between High and Low)

Maximum Bias Current: ±5 nA DC at 0 to 28 °C
±45 nA DC at 28 to 55 °C
(Current sourced by High or Low to Chassis into Input Terminals or back-plane, with isolation relays closed)

±1 nA DC at 0 to 55 °C
(Current sourced by High or Low to Chassis into back-plane, with isolation relays open)

Maximum Wire Size: 16 AWG

Ref. Junction Compensation Accuracy: 0.1 °C (over 18 to 28 °C operating temperature)

Max Temperature Difference Across Isothermal Module: 0.2 °C

*Applies to HP 3852As with firmware revision 2.0 or above.

10-19 HP 44711A AND HP 44713A PERFORMANCE TESTS

10-20 Introduction

The following Performance Tests check the operation of the HP 44711A and HP 44713A component module. Performance Tests are not given for the terminal modules. Successful completion of all tests in this chapter provides a high confidence level that the FET Multiplexer is meeting its listed specifications.

The Performance Tests should be performed in the order they are presented. The completion of each test increases the confidence level in FET Multiplexer operation. A minimum set of tests is given as Operational Verification Tests. These tests are described in Section 10-21.

The Performance Test procedures described in this chapter are involved and time consuming. Since the Operational Verification Tests yield a 90% confidence that the FET Multiplexer is operating normally, it is not recommended that all the Performance Tests be performed unless one of the tested specifications is in question.

10-21 Operational Verification

The first tests given in this section are the minimum set of tests recommended for the FET Multiplexer. These tests are designed to test the functionality and the on resistance of the FET switches. A ribbon cable test is included to verify that the HP 44711A or HP 44713A can communicate and transmit data over the ribbon cable to an HP 44702A/B. Successful completion of the Operational Verification Tests provides a 90% confidence level that the FET Multiplexer is operating normally and is within specification.

The Operational Verification Tests consist of the following:

Section 10-25 - Set-Up Procedure
Section 10-26 - Channel Switches Test
Section 10-27 - Tree Switch and Isolation Relay Test
Section 10-28 - Ribbon Cable Test

10-22 Equipment Required

The following test equipment is required to run the Performance Tests. Only the first four items in the list are required for the Operational Verification Tests.

1. Test Fixture (as described in Section 10-23)
2. Digital Multimeter -- HP 3456A or equivalent
3. HP 44702A/B High-Speed Voltmeter (for Ribbon Cable Test only)
4. Test Leads and Jumpers
5. Service Module -- HP 44743A
6. Resistor -- 10 Mohm
7. Resistor -- 1 kohm
8. Oscilloscope -- HP 1740A or equivalent (dual trace with delayed sweep)
9. +10 V Power Supply -- HP 6234 or equivalent

10. -10 V Power Supply -- HP 6234 or equivalent

NOTE

Except for the Ribbon Cable Test (it requires the HP 44702A/B), either of the accessory plug-in voltmeters (HP 44701A or HP 44702A/B) may be used for this test. This test does not describe the specific steps required to use the plug-in voltmeters. A description of the plug-in voltmeters can be found in the Plug-In Accessories Configuration and Programming Manual (HP part number 03852-90002).

10-23 Test Fixture

A test fixture is required to run the Performance Tests. A schematic of the required test fixture is shown in Figure 10-7a. A test fixture can be manufactured using an HP 44711AT terminal module (see Figure 10-7b). Because wiring the test fixture will make the terminal module unusable in an application, an additional terminal module should be ordered for service purposes.

If the test fixture is to be fabricated from other than an HP 44711AT terminal module, it is important that the terminal ID lines, shown in Figure 10-7a, be correctly wired. The HP 3852A local controller will not allow the execution of some commands with an incorrect terminal ID.

The test fixture consists of a short circuit between all channel HIGH lines and a short circuit between all channel LOW lines. The use of the test fixture minimizes the number of test lead connections required for the tests.

10-24 Test Procedures

WARNING

Even with power removed from the HP 3852A, high voltages, generated in other parts of the system, may be present at the terminal module of each accessory. Service personnel should ensure that all external power is removed from the system before installing, removing, testing or repairing any plug-in accessory.

10-25 Set-Up Procedure

1. Remove power from the HP 3852A.

2. Remove the terminal module from the rear of the FET multiplexer. Disconnect the ribbon cable if it is connected to either an HP 44702A/B or another FET multiplexer. Install the test fixture on the multiplexer. Note the slot number where the multiplexer under test is installed.

3. Verify the correct connections and slot numbers:

   a. Apply power to the HP 3852A. Wait for the HP 3852A to complete its wake-up sequence.

   b. Execute:

      ID? ES00 (where E = extender number, S = slot number)

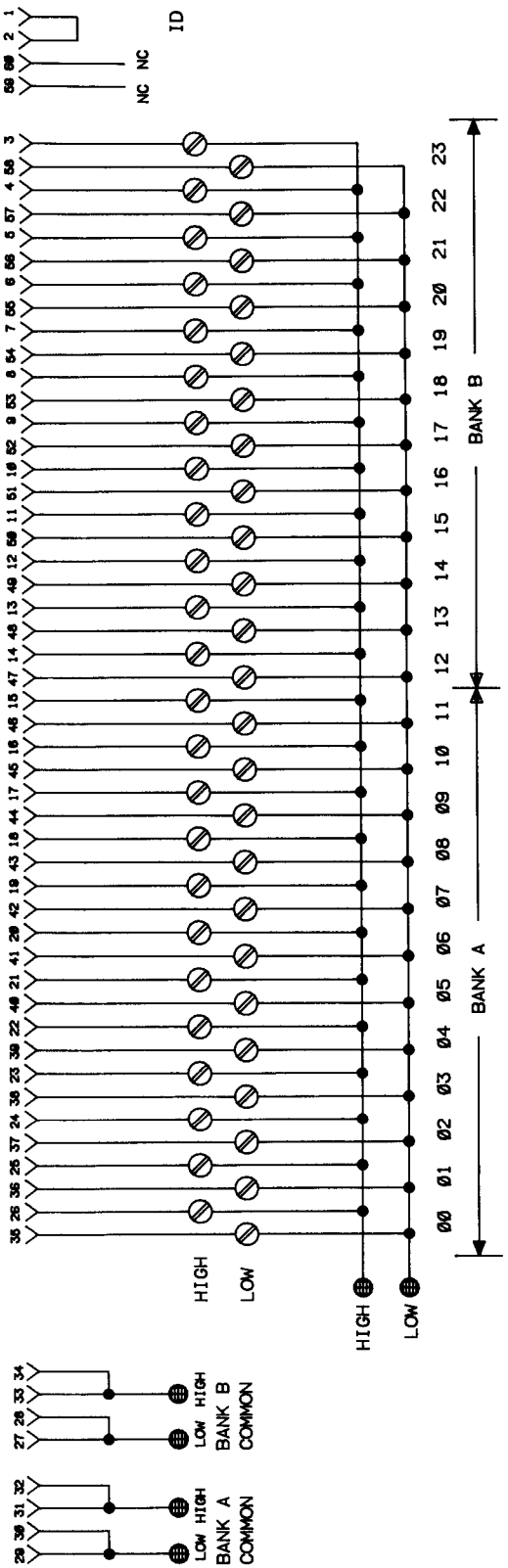


Figure 10-7a HP 44711A Test Fixure Schematic

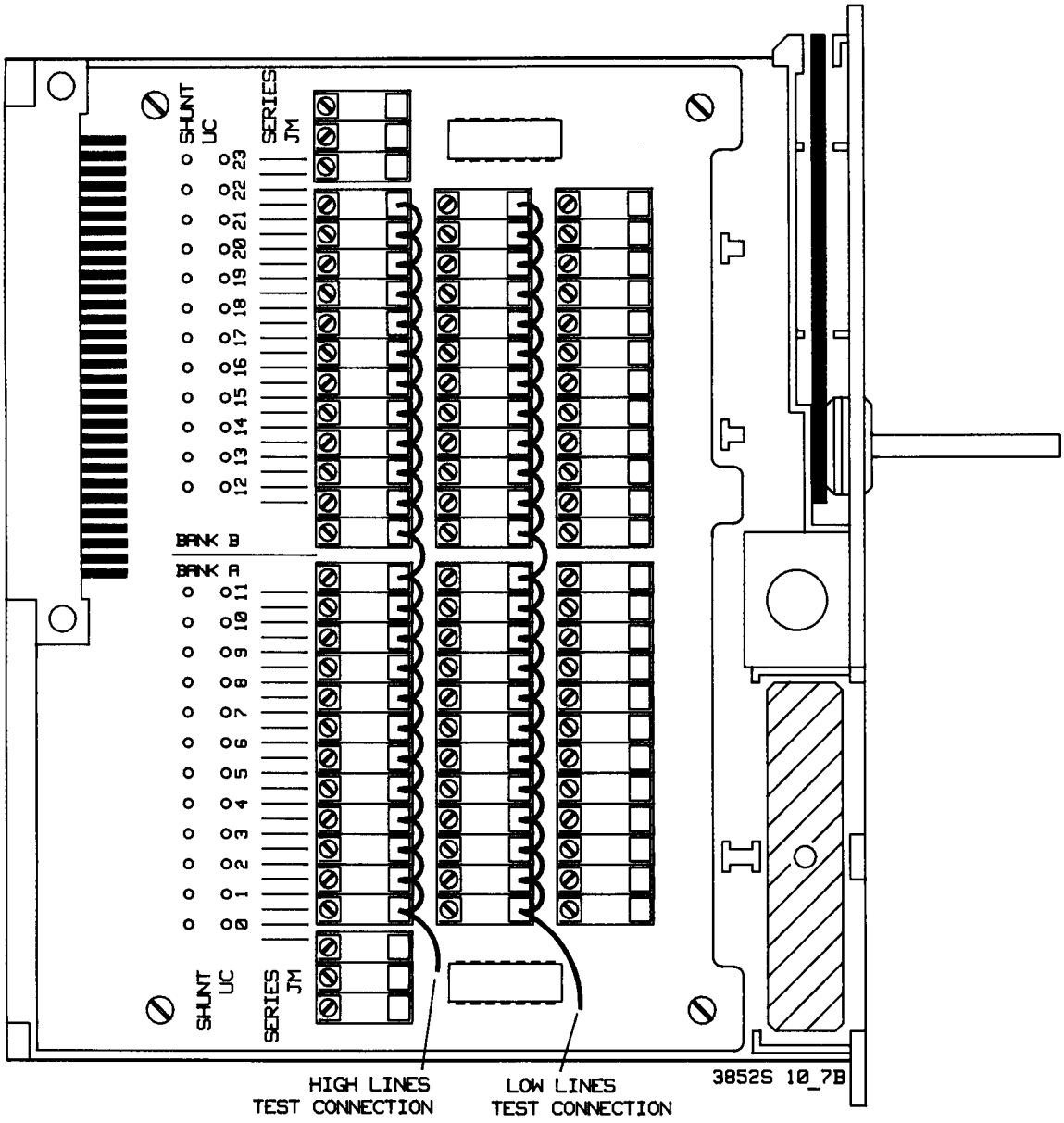


Figure 10-7b HP 44711A Test Fixure

c. Verify that the HP 3852A right display shows:

44711A

NOTE

If the HP 3852A right display shows a different accessory number, the slot number used may not be correct. If the HP 3852A display shows 447XXX, the test fixture is either not installed or the ID lines on the fixture are incorrectly wired.

10-26 Channel Switches Test

This test checks the on resistance for the HIGH and LOW FET switches in both Banks A and B.

1. Set the HP 44711A to a known state by executing:

RESET ES00 (where E = extender number, S = slot number)

This opens all switches on the HP 44711A.

2. On the test fixture, connect the multimeter DCV lead to the Bank A HIGH common test point. Connect the multimeter COM lead to the shorted HIGH connections of the channels. Short the Bank A and Bank B HIGH common test points together. Set the multimeter to measure two-wire ohms. The connections are shown in Figure 10-8.

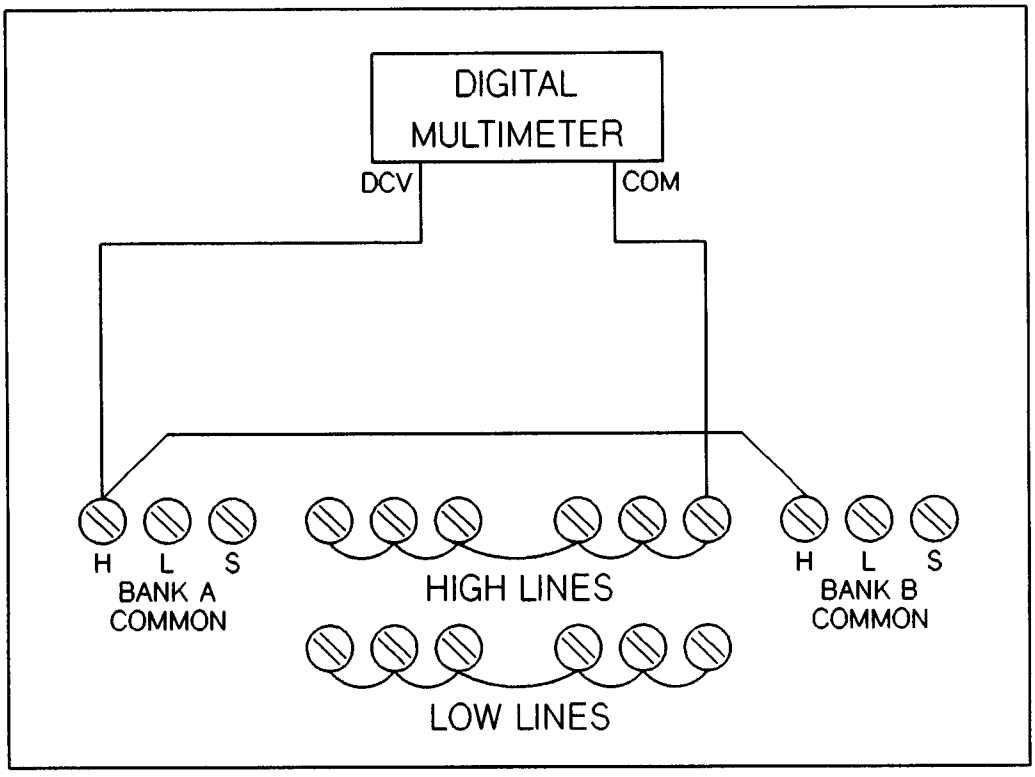


Figure 10-8 HP 44711A HIGH Channel Test Set-Up

3. Close the first channel by executing:

CLOSE ES00 (where E = extender number, S = slot number)

4. Observe the reading on the multimeter. The multimeter should indicate <1.6 kohms resistance. If the reading is greater than 1.6 kohms, the channel FET switch may be faulty.

5. Open the channel by executing:

OPEN ES00 (where E = extender number, S = slot number)

6. Observe the reading on the multimeter. The multimeter should indicate a resistance greater than 100 Mohm. It is important to perform this step to ensure that none of the FET switches are stuck on or leaking.

7. Repeat steps 4, 5, 6, and 7 for channels 01 through 23. In the CLOSE and OPEN commands the last two digits indicate the channel number. For example, CLOSE ES01 closes channel 01 in extender E at slot S.

8. Connect the multimeter DCV lead to the Bank A LOW common test point on the test fixture. Connect the multimeter COM lead to the shorted LOW connections of the channels. Short the Bank A and Bank B LOW common test points together. The connections are shown in Figure 10-9.

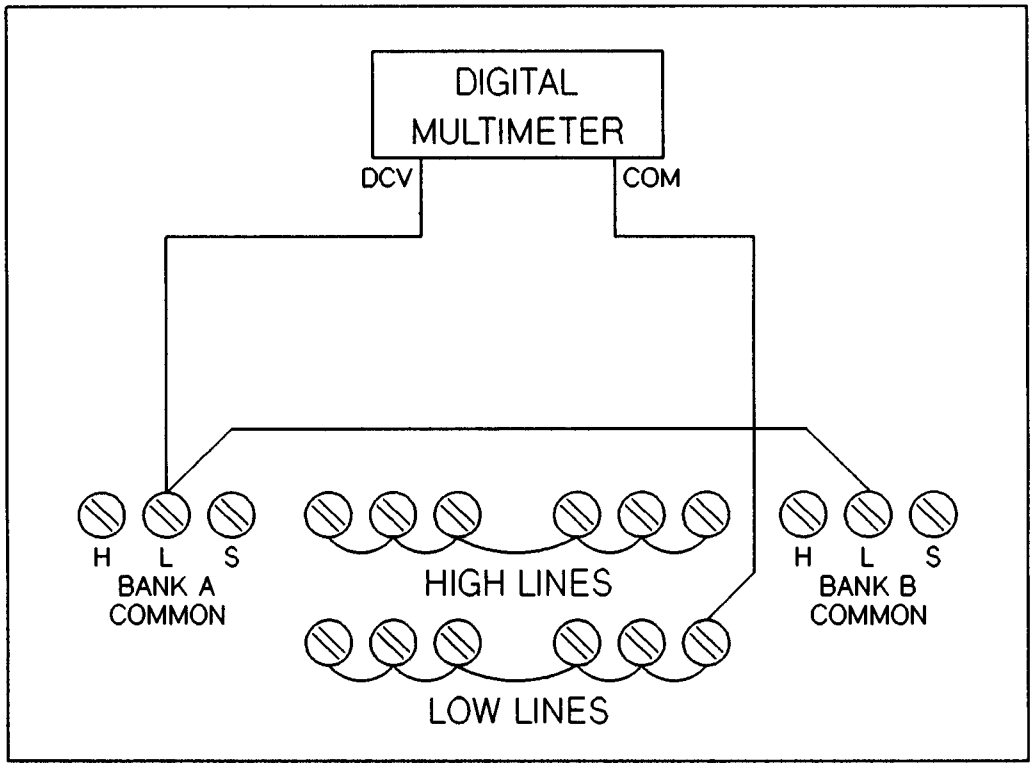


Figure 10-9 HP 44711A LOW Channel Test Set-Up

9. Repeat steps 3, 4, 5, 6, and 7. This checks the LOW path through the FET switches.

10-27 Tree Switch and Isolation Relay Test

1. SENSE BUS TREE SWITCH AND ISOLATION RELAY TEST: This test checks the measurement path from the backplane analog sense bus through the isolation relay and tree switches.

2. Connect a jumper between the Bank A common HIGH and Bank A common LOW connections on the test fixture.

3. Set the multimeter to measure two-wire ohms. Connect the multimeter test leads to the backplane analog bus sense HIGH and LOW lines.

NOTE

The backplane analog bus can be tested in one of two ways: 1) By connecting an external multimeter to the analog bus connector on the rear panel of the power supply module as shown in Figure 10-10, or 2) By connecting an external multimeter to the backplane analog bus line jumpers provided on the 44743A service module as shown in Figure 10-11.

4. Close Bank A sense tree switch and isolation relay by executing:

SWRITE ES00,6,-32608 (where E = extender number, S = slot number)

5. Observe the indication on the multimeter. The multimeter should indicate less than 3.2 kohm.

6. Open the tree switch and isolation relay by executing:

RESET ES00 (where E= extender number, S= slot number)

7. Observe the indication on the multimeter. The multimeter should indicate greater than 100 Mohm.

8. Disconnect the jumper between the Bank A common HIGH and the Bank A common low connection on the test fixure. Connect a jumper between the Bank B common HIGH and the Bank B common LOW connections on the test fixture.

9. Close the Bank B sense tree switch and isolation relay by executing:

SWRITE ES00,6,-32624 (where E = extender number, S = slot number)

10. Observe the indication on the multimeter. The multimeter should indicate less than 3.2 kohm.

11. Open the Bank B sense tree switch and isolation relay by executing:

RESET ES00 (where E= extender number, S= slot number)

12. Observe the indication on the multimeter. The multimeter should indicate greater than 100 Mohm.

13. SOURCE BUS TREE SWITCH AND ISOLATION RELAY TEST: This test checks the measurement path from the backplane analog source bus through the isolation relay and tree switches.

14. Set the multimeter to measure two-wire ohms. Connect the multimeter test leads to the backplane analog source bus HIGH and LOW lines.

15. Disconnect the jumper between the Bank B common HIGH and the Bank B common low connection on the test fixure. Connect a jumper between the Bank A common HIGH and the Bank A common LOW connections on the test fixture.

16. Close Bank A source tree switch and isolation relay by executing:

SWRITE ES00,6,-32672 (where E = extender number, S = slot number)

17. Observe the indication on the multimeter. The multimeter should indicate less than 3.2 kohm.

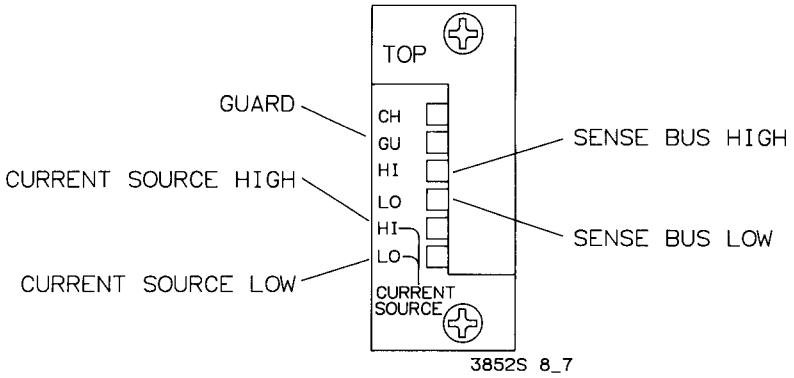


Figure 10-10 Analog Bus Connector

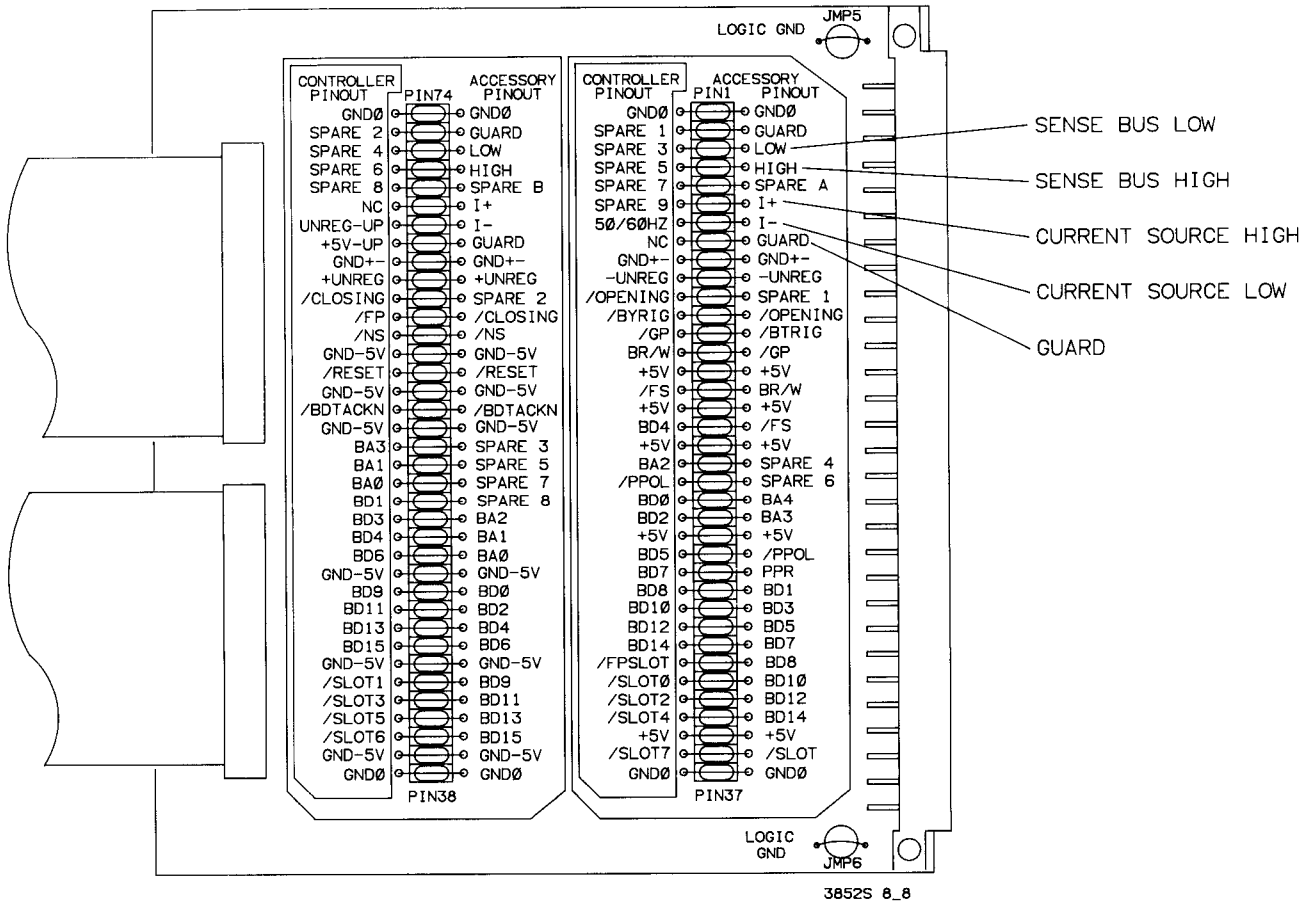


Figure 10-11 HP 44743A Service Module

18. Open the tree switch and isolation relay by executing:

RESET ES00 (where E = extender number, S = slot number)

19. Observe the indication on the multimeter. The multimeter should indicate greater than 100 Mohm.

20. Disconnect the jumper between the Bank A common HIGH and the Bank A common LOW connection on the test fixure. Connect a jumper between the Bank B common HIGH and the Bank B common LOW connections on the test fixture.

21. Close the Bank B source tree switch and isolation relay by executing:

SWRITE ES00,6,-32688 (where E = extender number, S = slot number)

22. Observe the indication on the multimeter. The multimeter should indicate less than 3.2 kohm.

23. Open the Bank B source tree switch and isolation relay by executing:

RESET ES00 (where E = extender number, S = slot number)

24. Observe the indication on the multimeter. The multimeter should indicate greater than 100 Mohm.

10-28 Ribbon Cable Test

This test verifies that the FET multiplexer can be controlled by the HP 44702A/B High-Speed Voltmeter. It also verifies that measurement results can be transferred to the voltmeter over the ribbon cable.

1. Remove power from the HP 3852A.

2. Install the HP 44711A component module in the mainframe next to an HP 44702A/B. Connect the ribbon cable between the FET multiplexer and the HP 44702A/B. Note the slot number where the FET under test is installed and the slot number where the HP 44702A/B is installed.

3. Install the test fixture on the FET multiplexer.

4. Apply power to the HP 3852A.

5. Set up the tests by executing the following commands:

```
USE ES00 (where E = extender number, S = slot number for High Speed Voltmeter)
FASTDISP OFF
SCANMODE ON
TERM RIBBON
```

6. On the test fixture, connect a jumper between the shorted HIGH lines and the shorted LOW lines.

7. Enter, but do not execute, the following command:

CONFMEAS OHM ES00-ES23 (where E = extender number, S = FET mux. slot number)

8. When the command entered in step 7 is executed, the HP 44702A/B will perform a resistance measurement on all channels on the HP 44711A. With the FASTDISP OFF, each measurement will appear in the HP 3852A right display. The HP 3852A left display will indicate each channel as it is scanned. Observe the HP 3852A displays and press execute. The resistance indicated in the right display, for all channels, should

be less than 6.2 kohms (the number in the display will be in exponential format). The resistance indicated includes the on-resistance of the channel FET switch, the on-resistance of the tree FET switch, and the resistance of the series protection resistors. The scan list can be repeated, if desired, by pressing the RECALL ENTRY key and then the ENTER key.

9. Remove the jumper from the test fixture.

10. Press the RECALL ENTRY key to retrieve the scan list command. Press the ENTER key and observe the displays. The resistance indicated in the HP 3852A right display should be infinite (the HP 44702A/B indicates an infinite resistance by the display: 1.000000E+38).

THIS CONCLUDES THE OPERATIONAL VERIFICATION PORTION OF THE HP 44711A/44713A PERFORMANCE TESTS.

10-29 DC Offset Test

1. Perform the Set-Up Procedure given in Section 10-25. The DC Offset test set-up is shown in Figure 10-12.

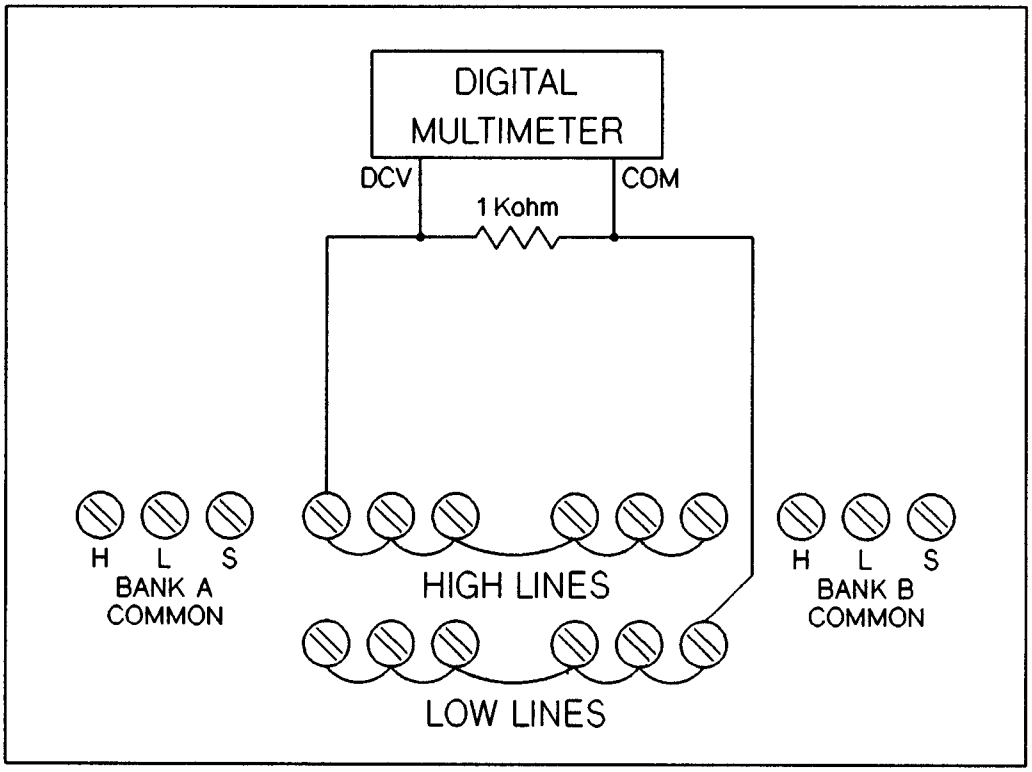


Figure 10-12 HP 44711A DC Offset Test Set-Up

2. Set the multimeter to measure DC volts, on a range with at least 10 μV resolution. Connect the multimeter DCV lead to the shorted HIGH lines of the test fixture. Connect the multimeter COM lead to the shorted LOW lines of the test fixture.

3. Connect the 1 kohm resistor across the multimeter input leads.

NOTE

The offset voltage is specified with a resistance of 1 kohm or less. A smaller value resistor may be used for this test.

4. Close the first channel in the multiplexer by executing:

CLOSE ES00 (where E = extender number, S = slot number)

5. Observe the indication on the multimeter. The voltage indicated should be less than 15 µV (0 to 28 °C) or less than 185 µV (28 to 55 °C). A failure of the DC Offset test indicates a failing channel FET switch.

6. Repeat steps 4 and 5 for channels 01 through 23. In the CLOSE command the last two digits are the channel number (i.e., CLOSE ES01 would close channel 01 in extender E at slot S).

10-30 Opening and Closing Time Set-Up Procedure

The Opening and Closing Time test verifies that the channel FETs will switch on and off and that the multiplexer can scan the channels at the specified speed.

1. Remove power from the HP 3852A and unplug the multiplexer to be tested. Install the Service Module in a convenient slot in the HP 3852A. Note the slot number where the Service Module is installed. Install the multiplexer on the service module. Install the test fixture on the multiplexer. The Set-Up Procedure is depicted in Figure 10-13.

2. On an oscilloscope, connect probes to the Channel A INPUT and the Channel B INPUT. Set up the oscilloscope to the following:

Dual Trace
Channel A – DC, 0.2 Volts/Div (if using 10:1 probes)
Channel B – DC, 0.5 Volts/Div (if using 10:1 probes)
Trigger – Internal, triggered on Channel B
Vertical Display – Alternate
Time – 0.5 mses/Div
Delayed Sweep – 0.1 µsec/Div
Delayed Sweep Dial – Minimum

3. Connect a jumper from the +5V test connection on the service module to the shorted HIGH connections on the test fixture.

4. Connect a jumper between the Bank A HIGH common test point and the Bank B HIGH common test point on the test fixure.

5. Connect the 1 kohm resistor between the HIGH common test points on the test fixture and the logic ground test connection on the service module.

6. Connect the Channel A oscilloscope probe to the HIGH common test points on the test fixture.

7. Connect the Channel B oscilloscope probe to the OPENING test connection on the service module.

8. Apply power to the HP 3852A. Wait for the wake-up sequence to complete.

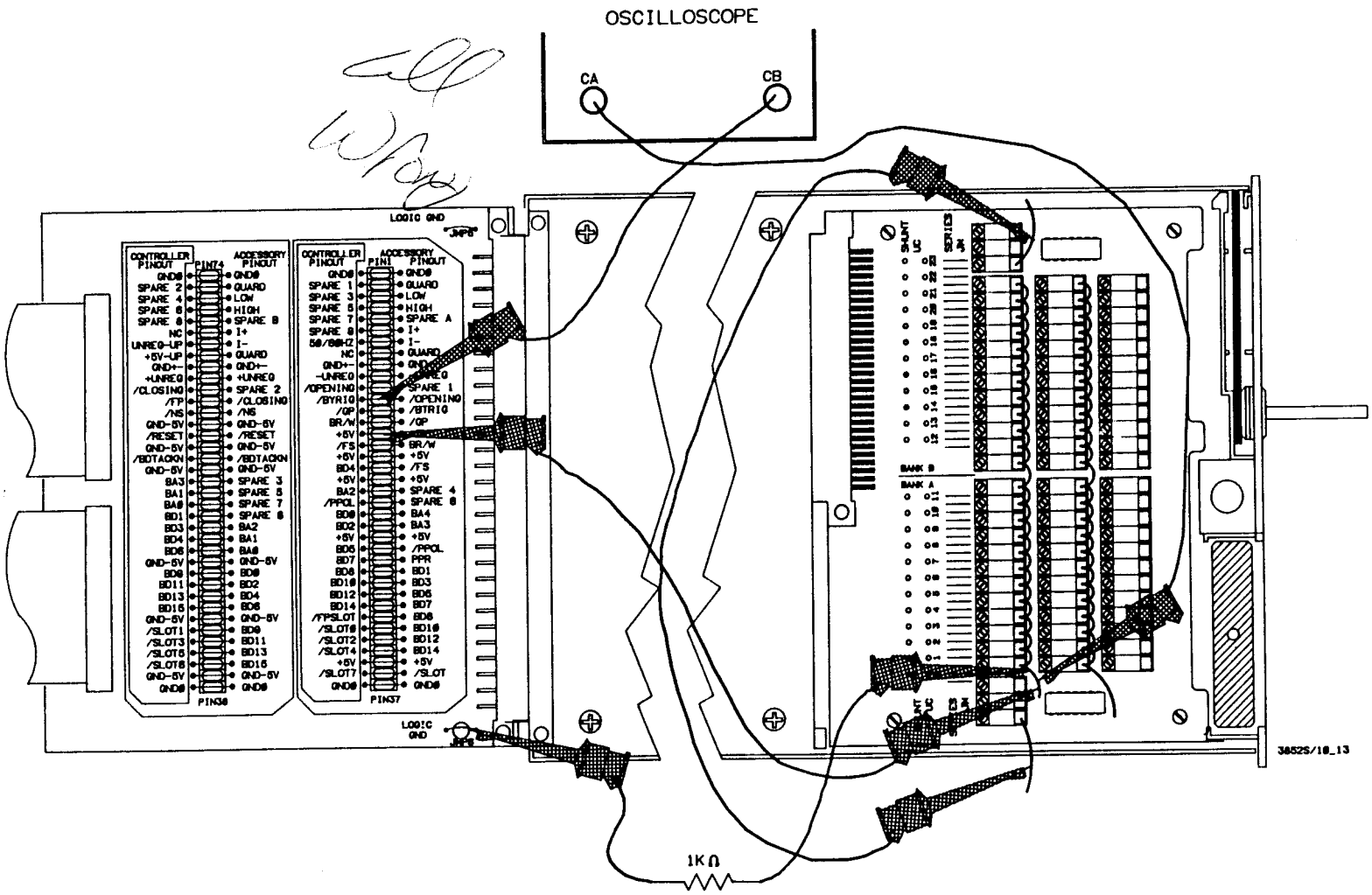
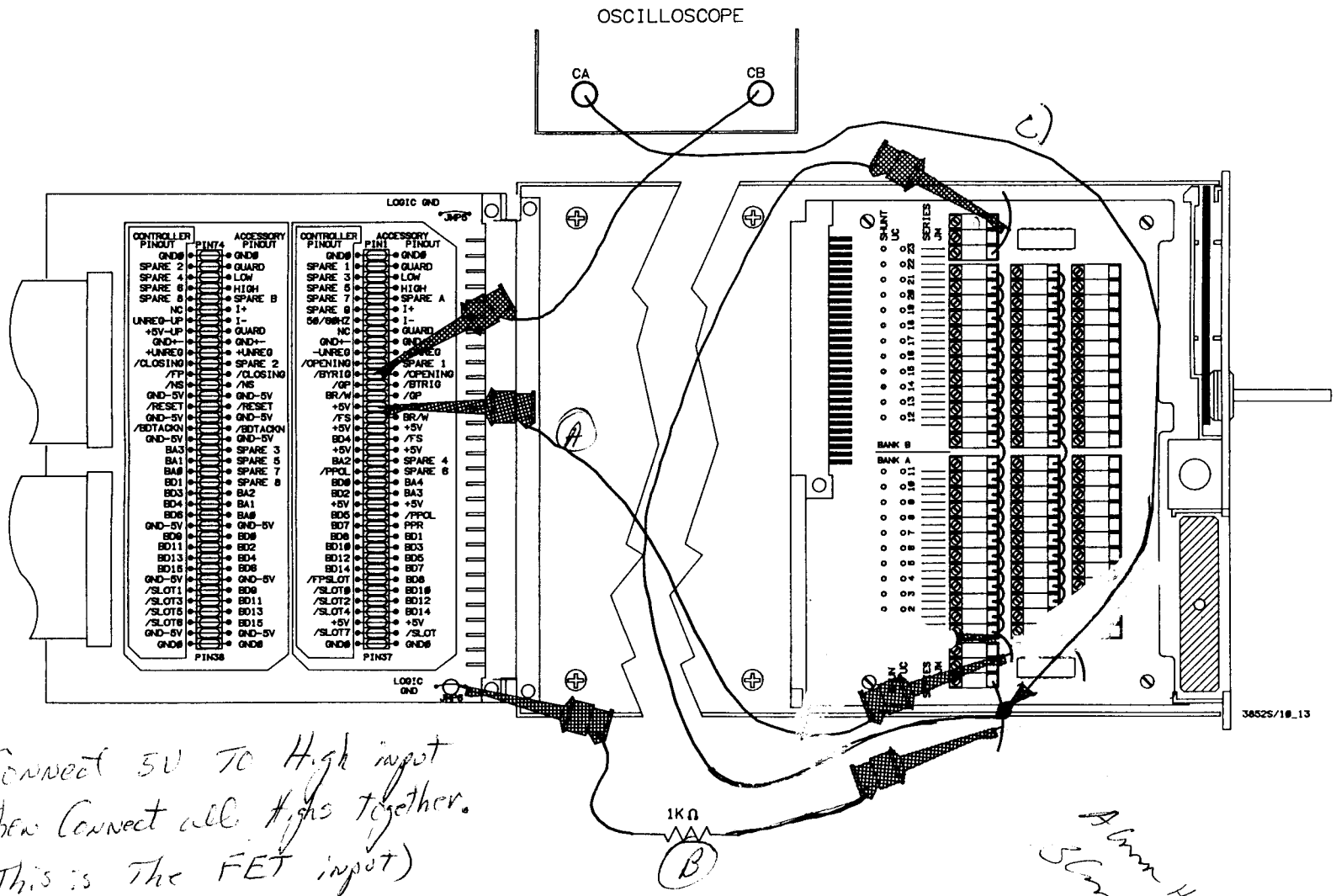


Figure 10-13 HP 44711A Opening Time Set-Up

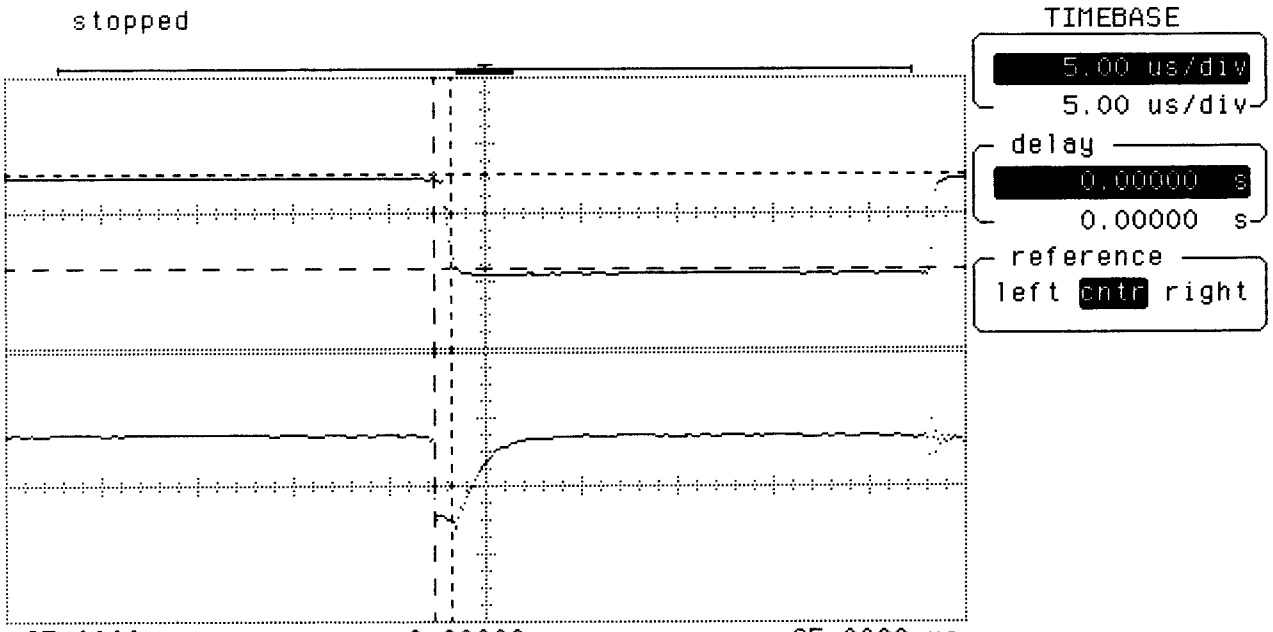


A) Connect 5V To High input
Then Connect all Highs together.
(This is The FET input)

B) Put a 1K To ground on
The common output. H

C) Probe The output

Figure 10-13 HP 44711A Opening Time Set-Up



Vmarker2(1)	2.87500 V	stop marker:	-1.80000us
Vmarker1(1)	125.000mV	start marker:	-2.70000us
delta V(1)	2.75000 V	delta t:	900.000ns
		1/delta t:	1.11111MHz

repetitive
realtime

	Sensitivity	Offset	Probe	Coupling	Impedance
Channel 1	2.00 V/div	1.75000 V	10:1	dc	1M ohm
Channel 2	400 mV/div	200.000 mV	10:1	dc	1M ohm

Trigger Mode: Edge
On the Positive Edge of Channel2
Trigger Level(s)
Channel2 = 296.000 mV (noise reject OFF)
HoldOff = 40.000 ns

9. Set up the following subroutine in HP 3852A memory. When the first statement is entered the SUB ENTRY annunciator should be on in the left display. This annunciator should remain on until the SUBEND statement is entered.

```
SUB A
TRG
SCAN ES00-ES23   (where E = extender number, S = slot number)
SUBEND
```

The subroutine will scan all channels on the FET multiplexer. Do not reset or cycle power to the HP 3852A or the subroutine will be erased from memory. The front panel CLEAR key may be used without disturbing the subroutine.

10-31 Opening Time Test

This test checks the time it takes for the FET to open after receiving an OPENING pulse from the FET multiplexer.

1. Repetitively call the entered subroutine 10000 times by executing:

```
CALL A,10000
```

This statement will call the subroutine 10000 times.

2. Observe the waveform displayed on the Channel B trace and make sure all 24 channels are present. It may also be necessary to adjust the TRIGGER LEVEL and TRIGGER HOLD controls, and to select the negative trigger pulse position on the scope to synchronize the signal on the scope.

3. Rotate the DELAY SWEEP dial to the minimum position. Select the DELAYED sweep mode on the scope. Slowly rotate the DELAY SWEEP dial clockwise while observing the displayed waveforms. The Channel B waveform is the OPENING pulse. The Channel A waveform is the +5V supply as switched by the relays. As the DELAY SWEEP dial is rotated, each channel switch and the associated OPENING pulse will come into view. The FET opening time is the time from the falling edge of the OPENING pulse to the falling edge of the Channel A waveform. This time must be less than 1.2 µseconds. The opening time is illustrated in Figure 10-14.

NOTE

The +5 V power supply waveform on Channel A will show an amplitude difference between the Bank A and Bank B FET switches. This is due to impedance differences in the Bank A common and Bank B common measurements paths on the multiplexer.

Continue rotating the DELAY Sweep dial until all 24 FET channels have been checked. A failing channel indicates a failing FET switch.

To stop the test at any time, press the front panel CLEAR key. The test time may be extended by increasing the number of times the subroutine is called, as specified in step 1.

The waveform will exhibit a small amount of jitter due to the overhead requirements of the HP 3852A operating system.

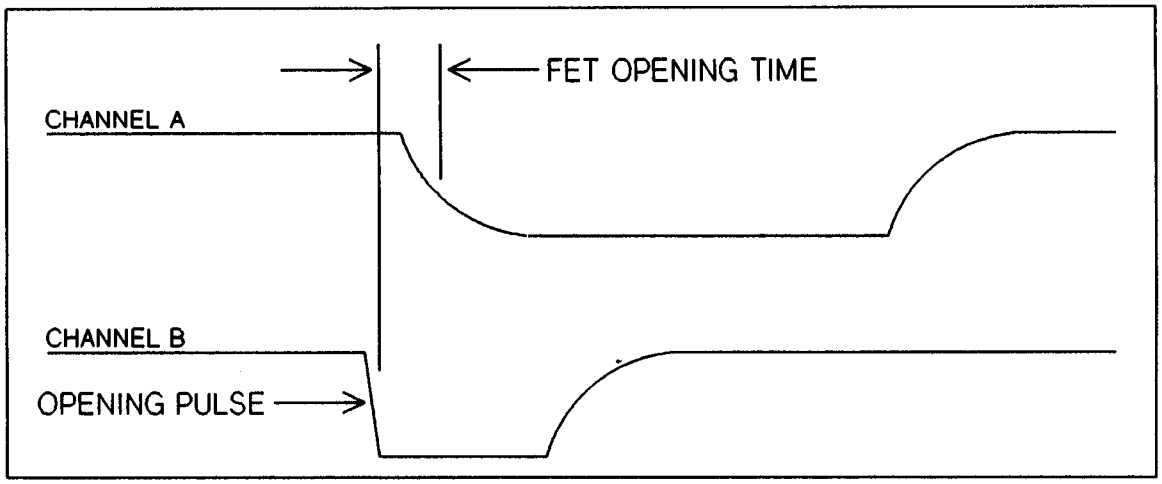


Figure 10-14 HP 44711A Opening Time

10-32 Closing Time Test

This test checks the time it takes for the FET to close after receiving a CLOSING pulse from the FET multiplexer.

1. Move the channel B oscilloscope probe to the CLOSING connection on the service module. The Closing Time test set-up is shown in Figure 10-15.

2. Repetitively call the entered subroutine by executing:

CALL A,10000

3. Rotate the DELAY SWEEP dial on the oscilloscope to the minimum position. Slowly rotate the dial clockwise until the first closing is displayed. The Channel B trace is the closing pulse output from the multiplexer. The Channel A waveform is the +5V supply, as switched by the FET channel switches. As the DELAY SWEEP dial is rotated, each channel switch and the associated CLOSING pulse will come into view. The FET closing time is the time from the falling edge of the CLOSING pulse to the rising edge of the Channel A waveform. This time must be less than 2.25 μseconds. The closing time is illustrated in Figure 10-16.

Continue rotating the DELAY Sweep dial until all 24 FET channels have been checked. A failing channel indicates a failing FET switch.

To stop the test at any time, press the front panel CLEAR key. The test time may be extended by by increasing the number of times the subroutine is called, as specified in step 2.

The waveform will exhibit a small amount of jitter due to the overhead requirements of the HP 3852A operating system.

10-33 Leakage/Bias Current Test

The leakage current test checks the FET switches for excessive leakage/bias current. Leakage/bias current is sourced by the multiplexer from HIGH or LOW to chassis ground.

1. OPEN CHANNELS LEAKAGE/BIAS CURRENT TEST. This test checks the leakage current with all channels open. A simplified schematic of the setup is shown in Figure 10-17 and the test setup for the HIGH lines is shown in Figure 10-18.

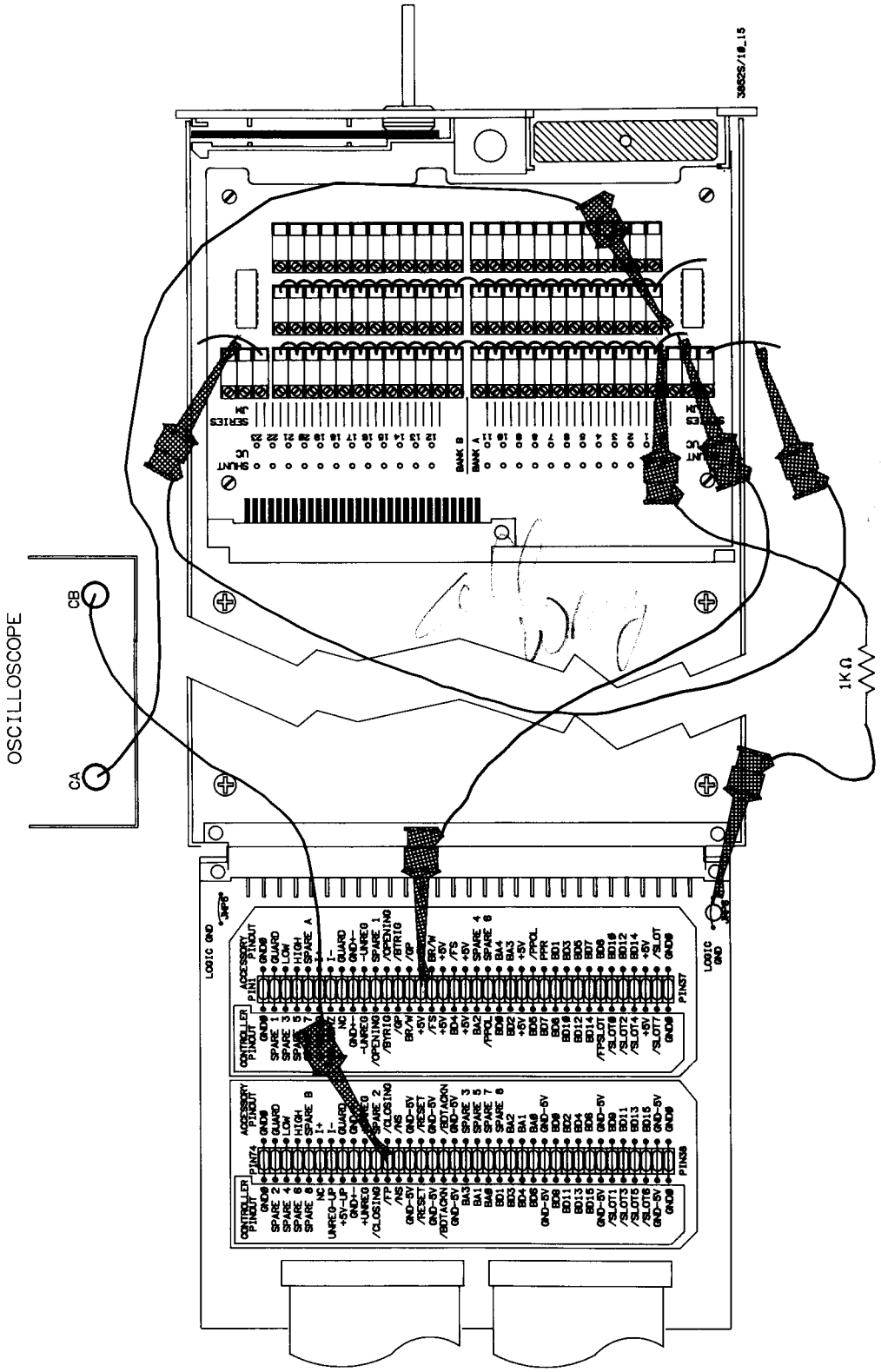


Figure 10-15 HP 44711A Closing Time Set-Up

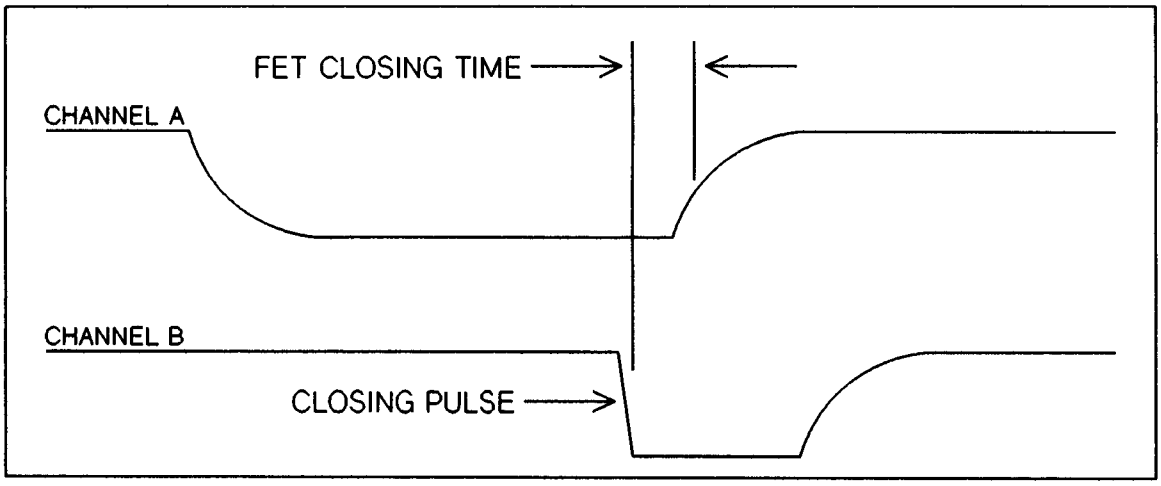


Figure 10-16 HP 44711A Closing Time

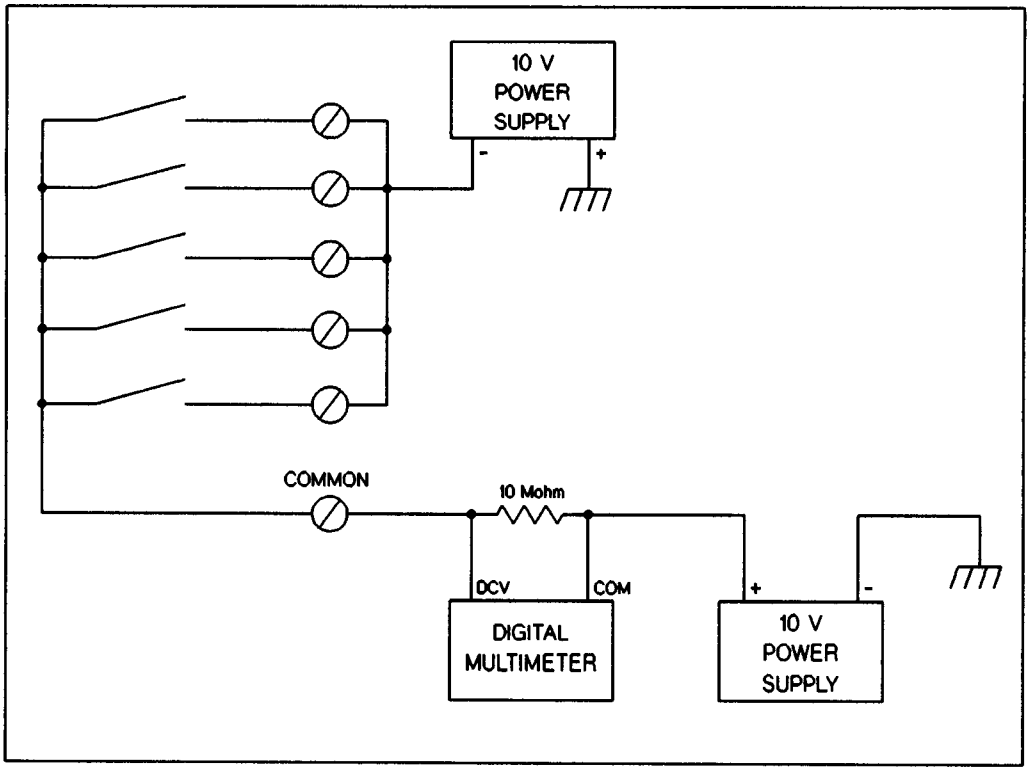


Figure 10-17 Open Channel Leakage Test

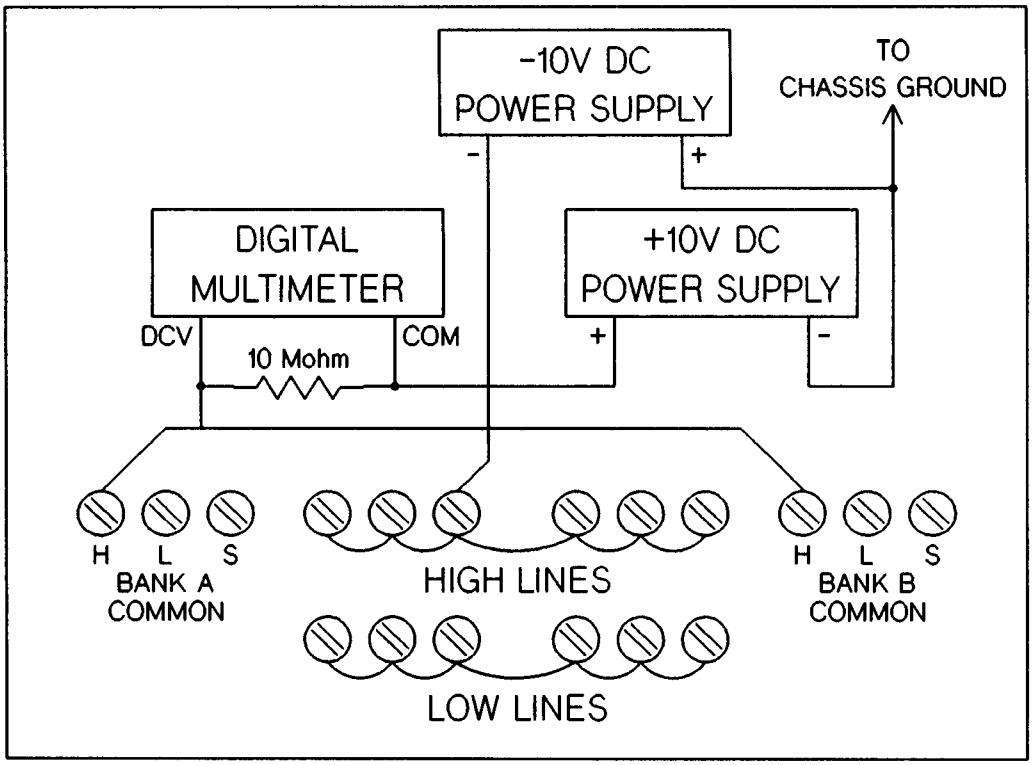


Figure 10-18 HP 44711A Open HIGH Channel Test Set-Up

2. Perform the Set-Up procedure in Section 10-23.

3. Set the negative power supply to 10 Vdc and connect the negative lead to the shorted HIGH lines on the test fixure. Connect the negative power supply common lead to the chassis.

NOTE

Connections to chassis ground can be accomplished by connecting to any sheet metal part. Chassis ground is also available at a connector on the rear panel of the HP 3852A power supply.

4. Set the positive power supply output to 10 Vdc and connect the positive lead to the multimeter common. Connect the positive power supply common to the chassis.

5. Connect the 10 Mohm resistor (**R1**) across the multimeter input terminals. Connect the multimeter DCV input terminal to the Bank A HIGH common test point. Short the Bank A and Bank B HIGH common test points together.

6. Open all switches on the multiplexer by executing:

RESET ES00 (where E = extender number, S = slot number)

7. Close the isolation relay and a tree switch by executing:

CLOSE ES90,ES94 (where E = extender number, S = slot number)

8. Observe the reading on the multimeter. This reading is referred to as **V1** in the following steps.

9. Calculate the leakage current (I) from the formula:

$$I = \frac{V1}{R1}$$

The calculated open channel leakage current for the HIGH lines should be less than 2 nA for a room temperature between 0° and 28° C (for temperatures in the range of 0° to 55° C the leakage current should be less than 11 nA).

10. Refer to Figure 10-19. Connect the negative power supply's negative lead to the shorted LOW lines on the test fixure. Connect the negative power supply common lead to the chassis.

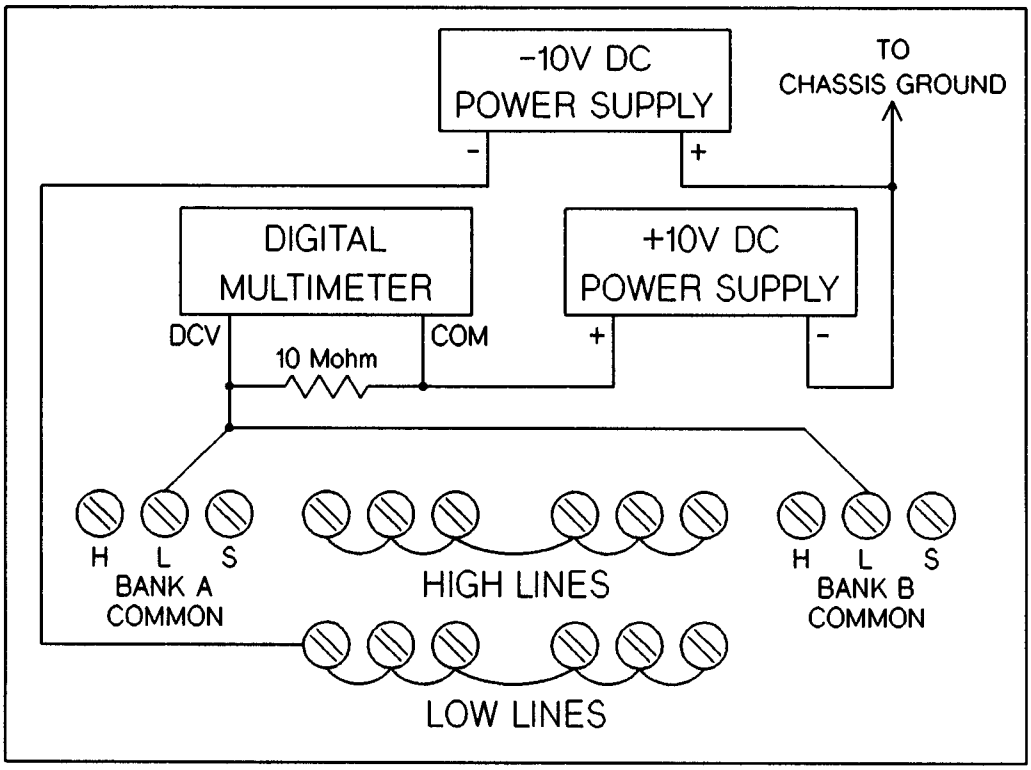


Figure 10-19 HP 44711A Open LOW Channel Test-Setup

11. Connect the multimeter DCV lead to the Bank A common LOW test point. Short the Bank A and Bank B LOW common test points together.

12. Observe the reading on the multimeter. This reading is referred to as **V1** in the following step.

13. Calculate the leakage current (I) from the formula:

$$I = \frac{V1}{R1}$$

The calculated open channel leakage current for the LOW lines should be less than 2 nA for a room temperature between 0° and 28° C (for temperatures in the range of 0° to 55° C the leakage current should be less than 11 nA).

14. CLOSED CHANNEL LEAKAGE/BIAS CURRENT TEST. This test checks each channel HIGH and LOW for leakage current when a channel is closed. A simplified schematic of the setup is shown in Figure 10-20 and the test setup for the HIGH lines is shown in Figure 10-21.

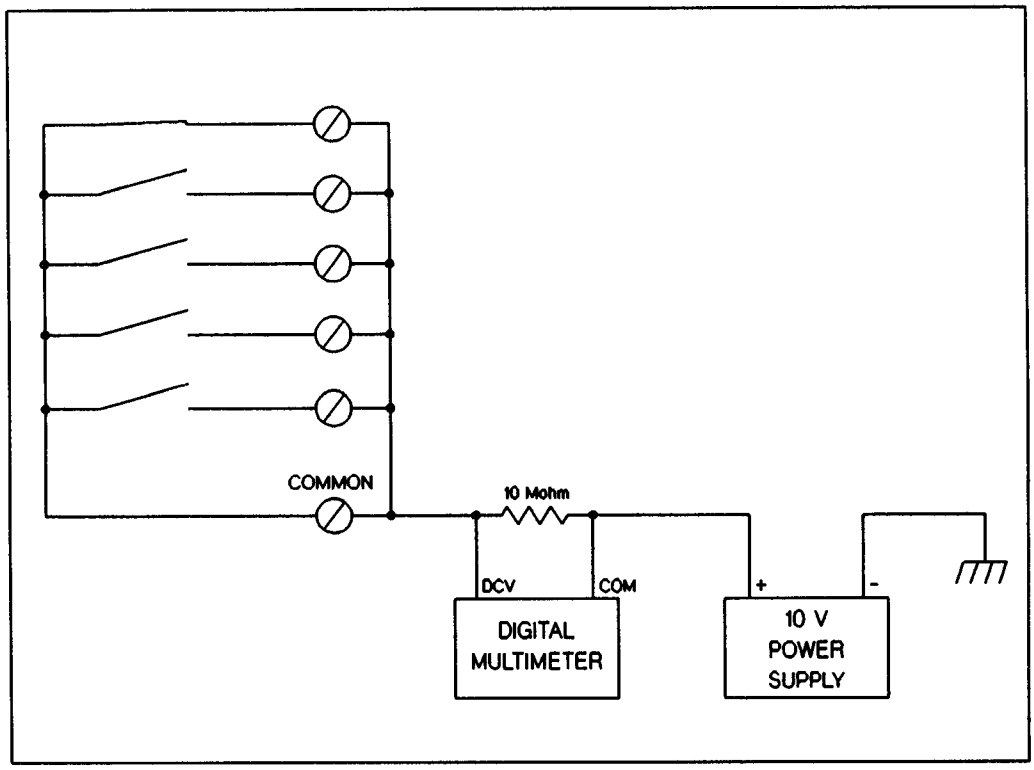


Figure 10-20 Closed Channel Leakage Test

15. Remove the negative power supply from the test fixure.

16. On the test fixture, connect the shorted HIGH lines to the Bank A HIGH common test point. Short the Bank A and Bank B common HIGH test points together.

17. Connect the +10 V power supply common to chassis ground. Connect the power supply positive lead to the common input of the multimeter.

18. Connect the 10 Mohm resistor across the multimeter input terminals. Connect the multimeter DCV input terminal to the shorted HIGH lines on the test fixture.

19. Close the isolation relay by executing:

CLOSE ES90 (where E = mainframe number, S = slot number)

20. Close the first channel in Bank A and the switch by executing:

CLOSE ES94,ES00 (where E = mainframe number, S = slot number)

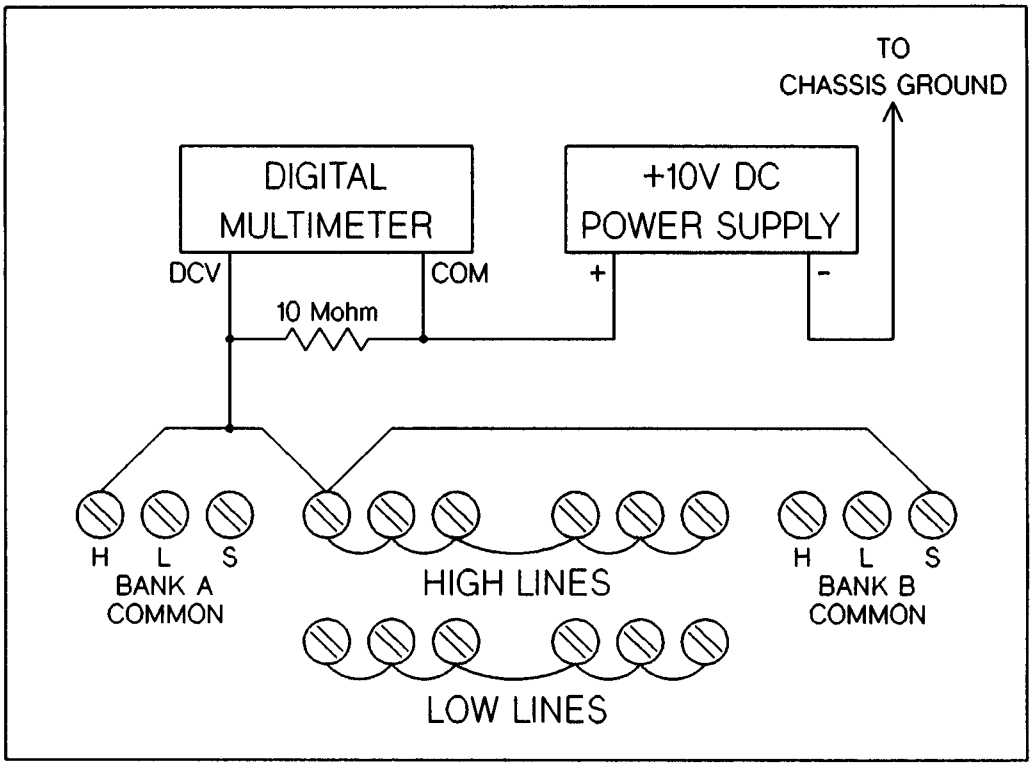


Figure 10-21 HP 44711A Closed HIGH Channel Test Set-Up

21. Observe the voltage reading on the multimeter. This voltage is referred to as **V1** in the following step.

22. Calculate the leakage current (I) from the formula:

$$I = \frac{V1}{R1}$$

The leakage current should be less than 5.0 nA for room temperatures in the range of 0° to 28° C (leakage current should be less than 15 nA for a temperature range of 28° to 55° C).

23. Repeat steps 24, 25, and 26 for channels 01 through 11. In step 21, the channel under test is specified in the second term of the CLOSE command (i.e., CLOSE ES94,ES01 for channel 01).

24. Close the first channel in Bank B and the tree switch by executing:

CLOSE ES94,ES12 (where E = mainframe number, S = slot number)

25. Observe the voltage reading on the multimeter. This voltage is referred to as **V1** in the following step.

26. Calculate the leakage current (I) from the formula:

$$I = \frac{V1}{R1}$$

The leakage current should be less than 5.0 nA for room temperatures in the range of 0° to 28° C (leakage current should be less than 15 nA for a temperature range of 28° to 55° C).

27. Repeat steps 24, 25, and 26 for channels 12 through 23. In step 24, the channel under test is specified in the second term of the CLOSE command (i.e., CLOSE ES92,ES11 for channel 11).

28. Refer to Figure 10-22. On the test fixture, connect the shorted LOW lines to the Bank A common LOW test point. Short the Bank A and Bank B LOW common test points together.

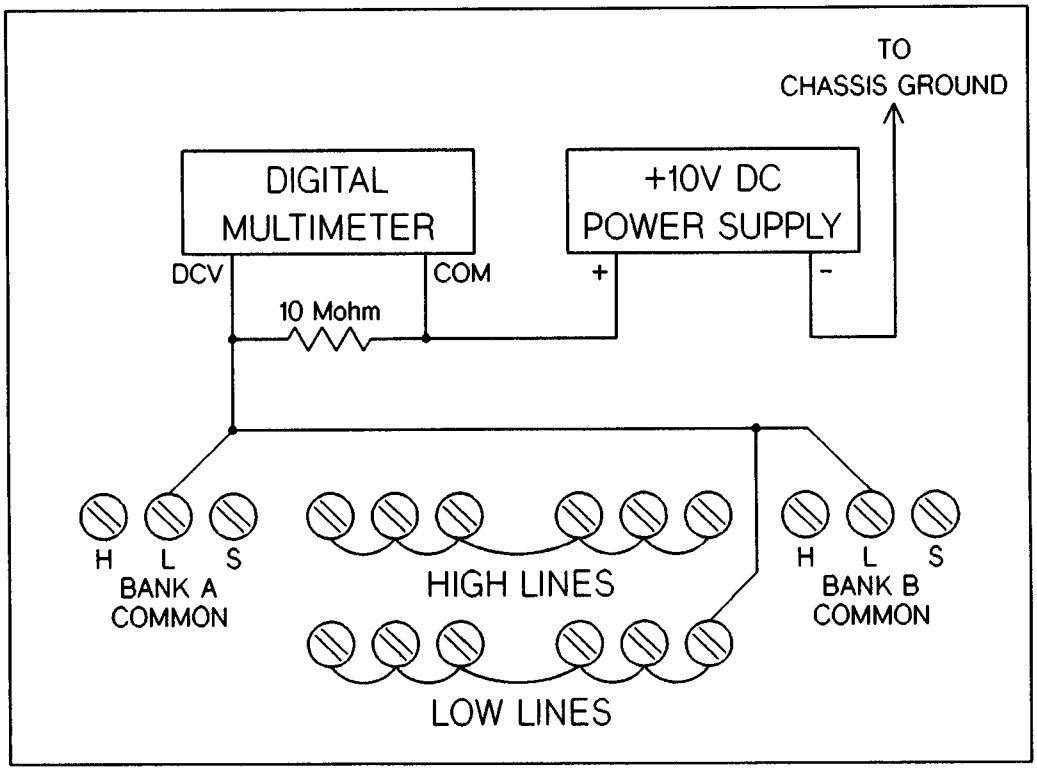


Figure 10-22 HP 44711A Closed LOW Channel Test Set-Up

29. Connect the multimeter DCV input terminal to the shorted LOW lines on the test fixture.

30. Close the first channel in Bank A and the tree switch by executing:

    CLOSE ES94,ES00 (where E = mainframe number, S = slot number)

31. Observe the voltage reading on the multimeter. This voltage is referred to as **V1** in the following step.

32. Calculate the leakage current (I) from the formula:

$$I = \frac{V1}{R1}$$

The leakage current should be less than 5.0 nA for room temperatures in the range of 0° to 28° C (leakage current should be less than 15 nA for a temperature range of 28° to 55° C).

33. Repeat steps 30, 31, and 32 for channels 01 through 11. In step 30, the channel under test is specified in the second term of the CLOSE command (i.e., CLOSE ES94,ES01 for channel 01).

34. Close the first channel in Bank B and the associated tree switch by executing:

CLOSE ES94,ES10 (where E = mainframe number, S = slot number)

35. Observe the voltage reading on the multimeter. This voltage is referred to as **V1** in the following step.

36. Calculate the leakage current (I) from the formula:

$$I = \frac{V1}{R1}$$

The leakage current should be less than 5.0 nA for room temperatures in the range of 0° to 28° C (leakage current should be less than 15 nA for a temperature range of 28° to 55° C).

37. Repeat steps 34, 35, and 36 for channels 12 through 23. In step 34, the channel under test is specified in the second term of the CLOSE command (i.e., CLOSE ES94,ES12 for channel 12).

10-34 HP 44712A PERFORMANCE TESTS

10-35 Introduction

The following Performance Tests check the operation of the HP 44712A component module. Performance Tests are not given for the terminal modules. Successful completion of all tests in this chapter provides a high confidence level that the FET Multiplexer is meeting its listed specifications.

The Performance Tests should be performed in the order they are presented. The completion of each test increases the confidence level in FET Multiplexer operation. A minimum set of tests is given as Operational Verification Tests. These tests are described in Section 10-36.

The Performance Test procedures described in this chapter are involved and time consuming. Since the Operational Verification Tests yield a 90% confidence that the FET Multiplexer is operating normally, it is not recommended that all the Performance Tests be performed unless one of the tested specifications is in question.

10-36 Operational Verification

The first tests given in this section are the minimum set of tests recommended for the FET Multiplexer. These tests are designed to test the functionality and the on resistance of the FET switches. A ribbon cable test is included to verify that the HP 44712A can communicate and transmit data over the ribbon cable to an HP 44702A/B. Successful completion of the Operational Verification Tests provides a 90% confidence level that the FET Multiplexer is operating normally and is within specification.

The Operational Verification Tests consist of the following:

Section 10-40 - Set-Up Procedure
Section 10-40 - Channel Switches Test
Section 10-42 - Tree Switch and Isolation Relay Test
Section 10-43 - Ribbon Cable Test

10-37 Equipment Required

The following test equipment is required to run the Performance Tests. Only the first four items in the list are required for the Operational Verification Tests.

1. Test Fixture (as described in Section 10-38)
2. Digital Multimeter -- HP 3456A or equivalent
3. HP 44702A/B High-Speed Voltmeter (for Ribbon Cable Test only)
4. Test Leads and Jumpers
5. Service Module -- HP 44743A
6. Resistor -- 10 Mohm
7. Resistor -- 1 kohm
8. Oscilloscope -- HP 1740A or equivalent (dual trace with delayed sweep)
9. +10 V Power Supply -- HP 6234 or equivalent

10. -10 V Power Supply -- HP 6234 or equivalent

NOTE

Except for the Ribbon Cable Test (it requires the HP 44702A/B), either of the accessory plug-in voltmeters (HP 44701A or HP 44702A/B) may be used for this test. This test does not describe the specific steps required to use the plug-in voltmeters. A description of the plug-in voltmeters can be found in the Plug-In Accessories Configuration and Programming Manual (HP part number 03852-90002).

10-38 Test Fixture

A test fixture is required to run the Performance Tests. A schematic of the required test fixture is shown in Figure 10-23a. A test fixture can be manufactured using an HP 44712AT terminal module (see Figure 10-23b). Because wiring the test fixture will make the terminal module unusable in an application, an additional terminal module should be ordered for service purposes.

If the test fixture is to be fabricated from other than an HP 44712AT terminal module, it is important that the terminal ID lines, shown in Figure 10-23a, be correctly wired. The HP 3852A local controller will not allow the execution of some commands with an incorrect terminal ID.

The test fixture consists of a short circuit between all channel HIGH lines and test connections for the LOW line. The use of the test fixture minimizes the number of test lead connections required for the tests.

10-39 Test Procedures

WARNING

Even with power removed from the HP 3852A, high voltages, generated in other parts of the system, may be present at the terminal module of each accessory. Service personnel should ensure that all external power is removed from the system before installing, removing, testing or repairing any plug-in accessory.

10-40 Set-Up Procedure

1. Remove power from the HP 3852A.

2. Remove the terminal module from the rear of the FET multiplexer. Disconnect the ribbon cable if it is connected to either an HP 44702A/B or another FET multiplexer. Install the test fixture on the multiplexer. Note the slot number where the multiplexer under test is installed.

3. Verify the correct connections and slot numbers:

   a. Apply power to the HP 3852A. Wait for the HP 3852A to complete its wake-up sequence.

   b. Execute:

      ID? ES00 (where E = extender number, S = slot number)

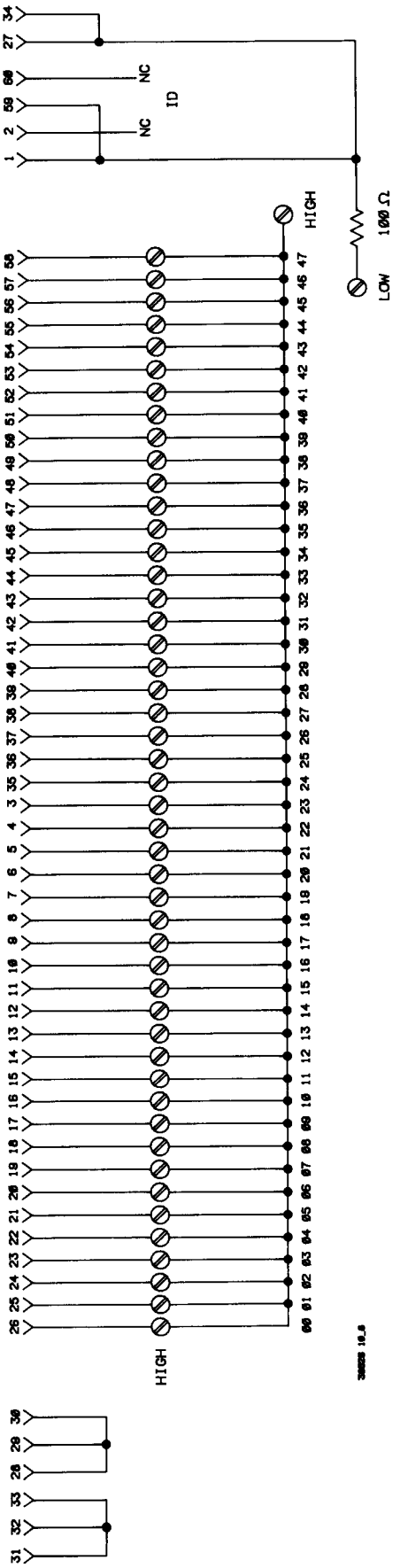


Figure 10-23a HP 44712A Test Fixure Schematic

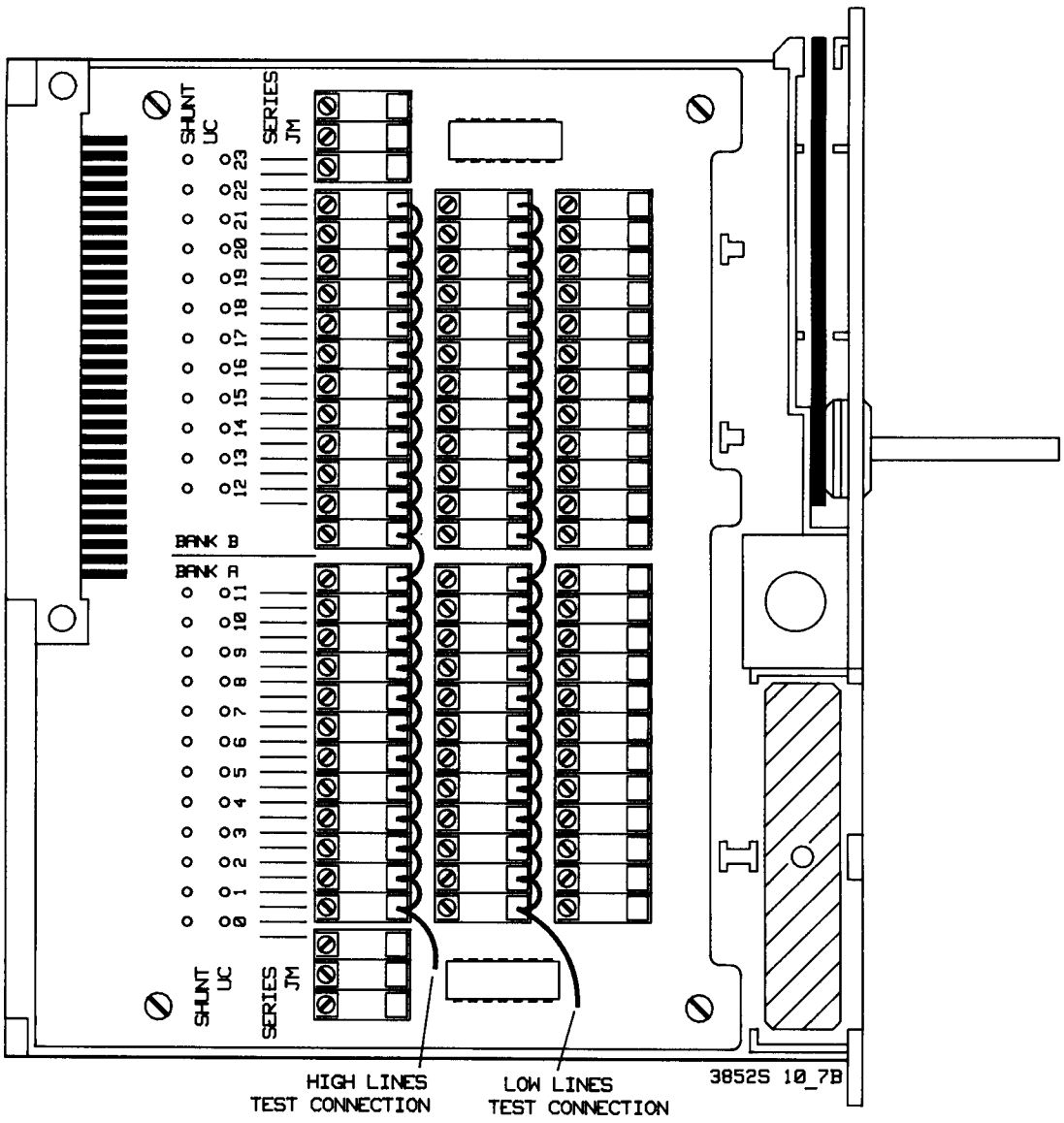


Figure 10-23b HP 44712A Test Fixure

c. Verify that the HP 3852A right display shows:

44712A

NOTE

If the HP 3852A right display shows a different accessory number, the slot number used may not be correct. If the HP 3852A display shows 447XXX, the test fixture is either not installed or the ID lines on the fixture are incorrectly wired.

10-41 Channel and Sense Bus Tree Switches, and Isolation Relay Test

This test checks the measurement path from each channel input to the HP 3852A backplane analog sense bus.

1. Set the HP 44712A to a known state by executing:

    RESET ES00 (where E = extender number, S = slot number)

This opens all switches on the HP 44712A.

2. Set the multimeter to measure two-wire ohms. Connect the multimeter DCV lead to the backplane analog bus sense HIGH line. Connect the multimeter COM lead to the backplane analog bus sense LOW line.

NOTE

The backplane analog bus can be tested in one of two ways: 1) By connecting an external multimeter to the analog bus connector on the rear panel of the power supply module as shown in Figure 10-24, or 2) By connecting an external multimeter to the backplane analog bus line jumpers provided on the 44743A service module as shown in Figure 10-25.

3. Connect a jumper between the shorted HIGH lines and the shorted LOW lines on the test fixure.

4. Close the first channel by executing:

    CLOSE ES90,ES92,ES00 (where E = extender number, S = slot number)

5. Observe the reading on the multimeter. The multimeter should indicate <4.6 kohms resistance. If the reading is greater than 4.6 kohms, the channel FET switch or sense bus tree switch FET, or isolation relay may be faulty.

6. Open the channel by executing:

    OPEN ES90,ES92,ES00 (where E = extender number, S = slot number)

7. Observe the reading on the multimeter. The multimeter should indicate greater than 100 Mohm.

8. Repeat steps 4, 5, 6, and 7 for channels 01 through 47. In the CLOSE and OPEN commands the last two digits indicate the channel number. For example, CLOSE ES01 closes channel 01 in extender E at slot S. Note that in steps 3 and 5 the isolation relays and tree FET switches are controlled by using channel numbers 90 and 92, respectively. These two channels must remain the same for all channels tested in this test.

10-42 Source Bus Tree Switches Test

This test checks the measurement path from the backplane analog source bus through the isolation relay and tree switches. Only two channels are used for the test since all channel switches should be tested by the previous test in Section 10-41.

1. Set the multimeter to measure two-wire ohms. Connect the multimeter DCV lead to the backplane analog bus source HIGH line. Connect the multimeter COM lead to the backplane analog bus source LOW line.

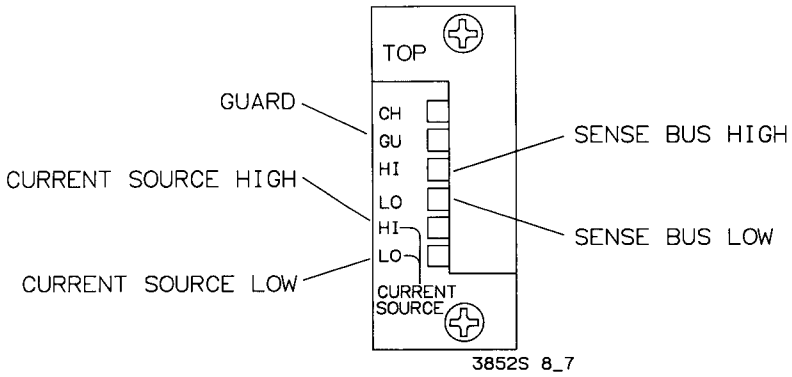


Figure 10-24 Analog Bus Connector

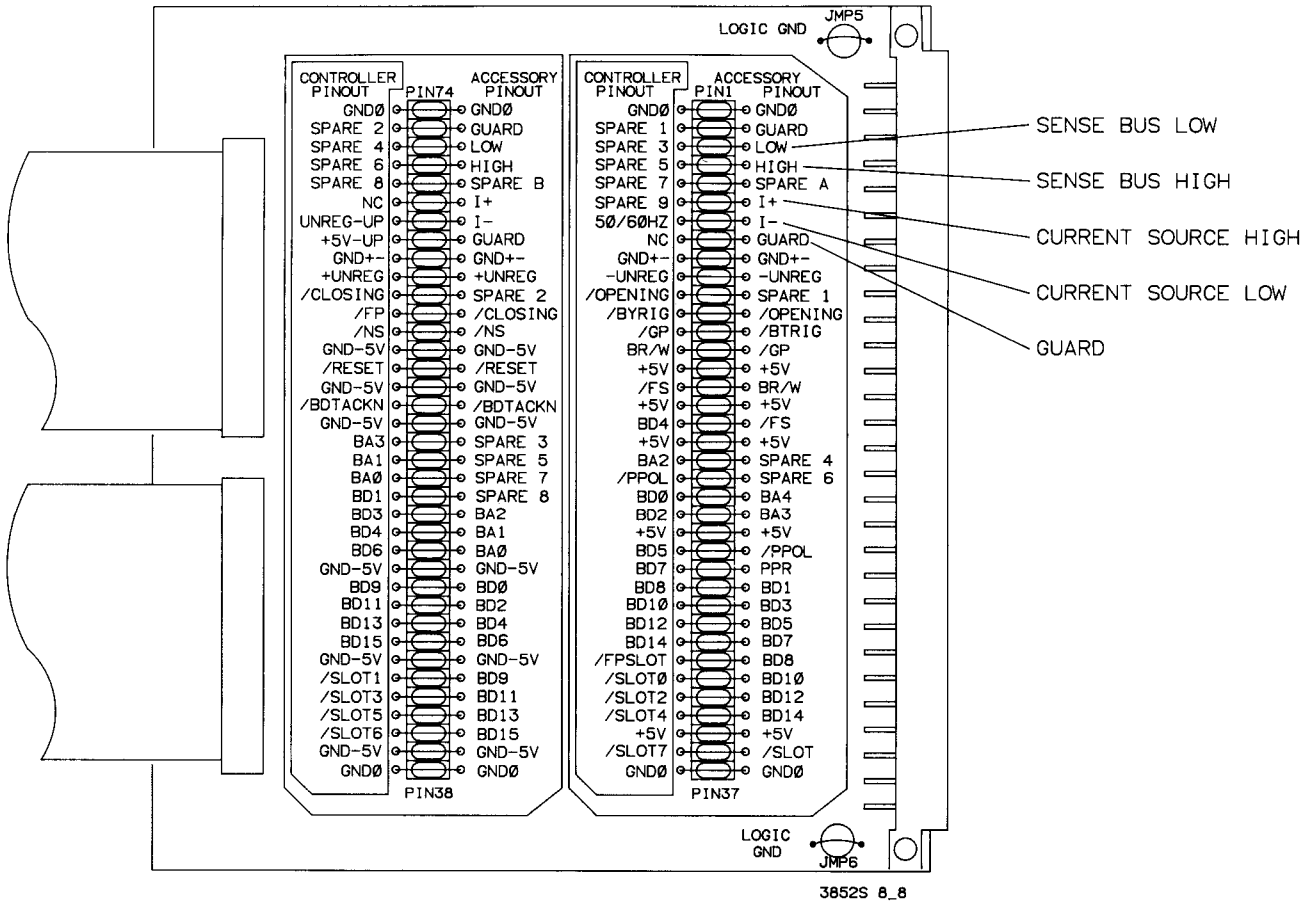


Figure 10-25 HP 44743A Service Module

2. Connect a jumper between the shorted HIGH lines and the shorted LOW lines on the test fixure.

3. Close the first channel by executing:

CLOSE ES90,ES91,ES00 (where E = extender number, S = slot number)

4. Observe the reading on the multimeter. The multimeter should indicate <4.6 kohms resistance. If the reading is greater than 4.6 kohms, the source bus tree switch FET may be faulty.

5. Open the channel by executing:

OPEN ES90,ES91,ES00 (where E = extender number, S = slot number)

6. Observe the reading on the multimeter. The multimeter should indicate greater than 100 Mohm.

7. Close channel 24 by executing:

CLOSE ES90,ES91,ES24 (where E = extender number, S = slot number)

8. Observe the reading on the multimeter. The multimeter should indicate <4.6 kohms resistance.

9. Open the channel by executing:

OPEN ES90,ES91,ES00 (where E= extender number, S= slot number)

10. Observe the reading on the multimeter. The multimeter should indicate greater than 100 Mohm.

10-43 Ribbon Cable Test

This test verifies that the FET multiplexer can be controlled by the HP 44702A/B High-Speed Voltmeter. It also verifies that measurement results can be transferred to the voltmeter over the ribbon cable.

1. Remove power from the HP 3852A.

2. Install the HP 44712A component module in the mainframe next to an HP 44702A/B. Connect the ribbon cable between the FET multiplexer and the HP 44702A/B. Note the slot number where the FET under test is installed and the slot number where the HP 44702A/B is installed.

3. Install the test fixture on the FET multiplexer.

4. Apply power to the HP 3852A.

5. Set up the tests by executing the following commands:

```
USE ES00 (where E = extender number, S = slot number for High Speed Voltmeter)
FASTDISP OFF
SCANMODE ON
TERM RIBBON
```

6. On the test fixture, connect a jumper between the shorted HIGH lines and the shorted LOW lines.

7. Enter, but do not execute, the following command:

CONFMEAS OHM ES00-ES23 (where E = extender number, S = FET mux. slot number)

8. When the command entered in step 7 is executed, the HP 44702A/B will perform a resistance measurement on all channels on the HP 44712A. With the FASTDISP OFF, each measurement will appear in the HP 3852A right display. The HP 3852A left display will indicate each channel as it is scanned. Observe the HP 3852A displays and press execute. The resistance indicated in the right display, for all channels, should be less than 4.6 kohms (the number in the display will be in exponential format). The resistance indicated includes the on-resistance of the channel FET switch, the on-resistance of the tree FET switch, and the resistance of the series protection resistor. The scan list can be repeated, if desired, by pressing the RECALL ENTRY key and then the ENTER key.

9. Remove the jumper from the test fixture.

10. Press the RECALL ENTRY key to retrieve the scan list command. Press the ENTER key and observe the displays. The resistance indicated in the HP 3852A right display should be infinite (the HP 44702A/B indicates an infinite resistance by the display: 1.000000E+38).

THIS CONCLUDES THE OPERATIONAL VERIFICATION PORTION OF THE HP 44712A PERFORMANCE TESTS.

10-44 DC Offset Test

1. Perform the Set-Up Procedure given in Section 10-40. The DC Offset test set-up is shown in Figure 10-26.

2. Set the multimeter to measure DC volts, on a range with at least 10 µV resolution. Connect the multimeter DCV lead to the shorted HIGH lines of the test fixture. Connect the multimeter COM lead to the LOW lines of the test fixture.

3. Connect the 1 kohm resistor across the multimeter input leads.

NOTE

The offset voltage is specified with a resistance of 1 kohm or less. A smaller value resistor may be used for this test.

4. Close the first channel in the multiplexer by executing:

CLOSE ES00 (where E = extender number, S = slot number)

5. Observe the indication on the multimeter. The voltage indicated should be less than 15 µV (0 to 28 °C) or less than 185 µV (28 to 55 °C). A failure of the DC Offset test indicates a failing channel FET switch.

6. Repeat steps 4 and 5 for channels 01 through 47. In the CLOSE command the last two digits are the channel number (i.e., CLOSE ES01 would close channel 01 in extender E at slot S).

10-45 Opening and Closing Time Set-Up Procedure

The Opening and Closing Time test verifies that the channel FETs will switch on and off and that the multiplexer can scan the channels at the specified speed.

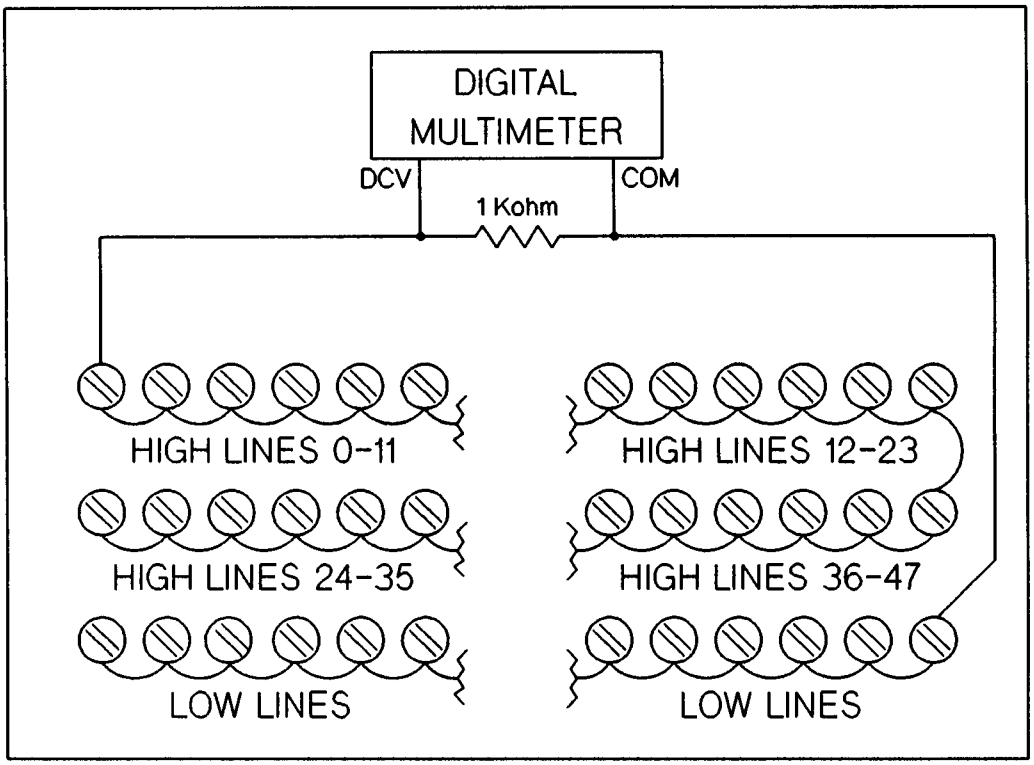


Figure 10-26 HP 44712A DC Offset Test Set-Up

1. Remove power from the HP 3852A and unplug the multiplexer to be tested. Install the Service Module in a convenient slot in the HP 3852A. Note the slot number where the Service Module is installed. Install the multiplexer on the service module. Install the test fixture on the multiplexer. The Set-Up Procedure is depicted in Figure 10-27.

2. On an oscilloscope, connect probes to the Channel A INPUT and the Channel B INPUT. Set up the oscilloscope to the following:

Dual Trace
Channel A -- DC, 0.2 Volts/Div (if using 10:1 probes)
Channel B -- DC, 0.5 Volts/Div (if using 10:1 probes)
Trigger -- Internal, triggered on Channel B
Vertical Display -- Alternate
Time -- 0.5 mses/Div
Delayed Sweep -- 0.1 µsec/Div
Delayed Sweep Dial -- Minimum

3. Connect the 1 kohm resistor between the analog bus sense HIGH connection and the +5 V connection on the service module.

4. Connect a jumper between the analog bus sense LOW connection and the logic ground test point on the service module.

5. Connect the shorted HIGH lines to the shorted LOW lines on the test fixure.

6. Connect the Channel A oscilloscope probe to the analog bus sense HIGH connection on the service module.

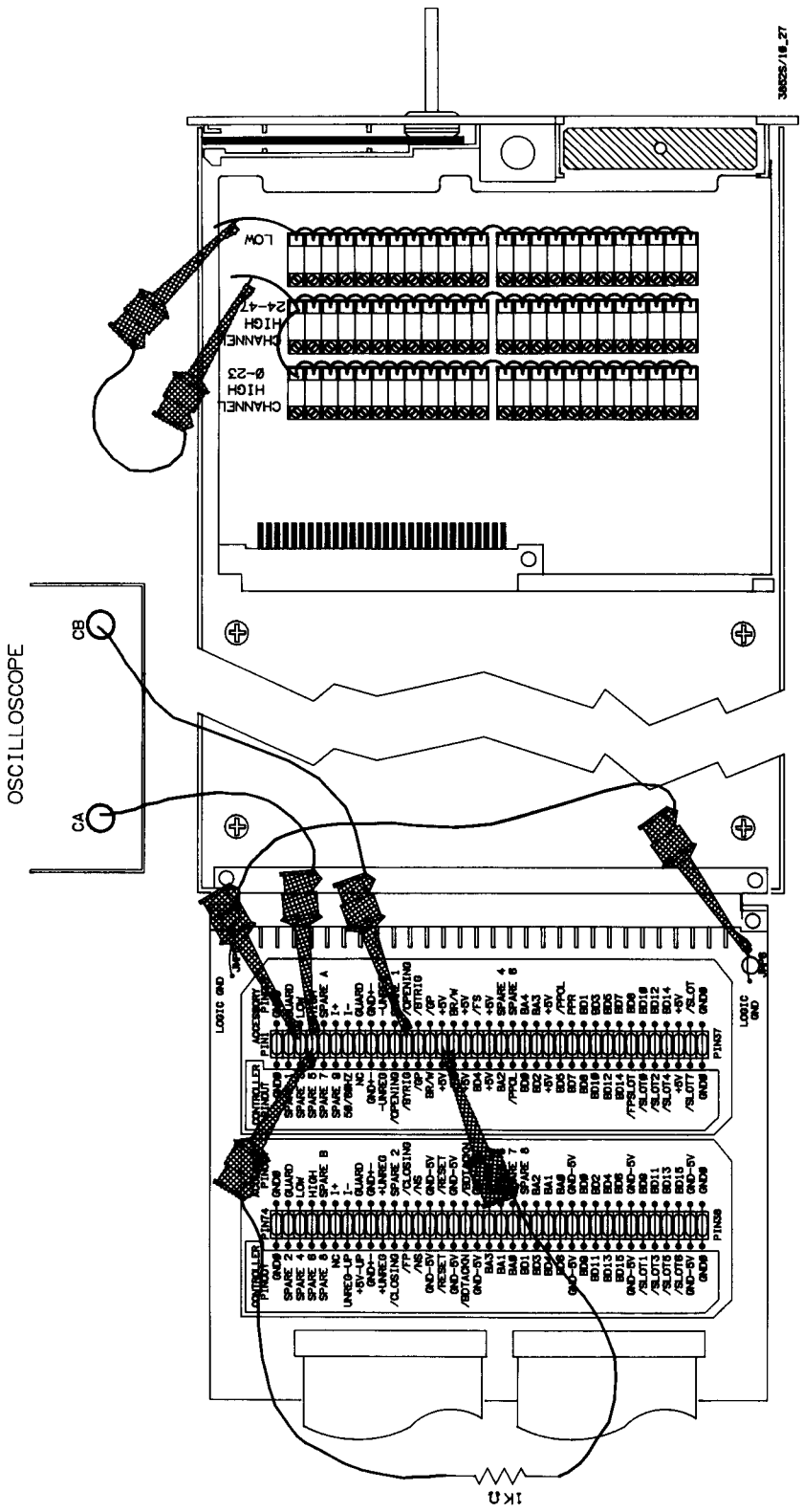


Figure 10-27 HP 44712A Opening Time Set-Up

7. Connect the Channel B oscilloscope probe to the OPENING test connection on the service module.

8. Apply power to the HP 3852A. Wait for the wake-up sequence to complete.

9. Set up the following subroutine in HP 3852A memory. When the first statement is entered the SUB ENTRY annunciator should be on in the left display. This annunciator should remain on until the SUBEND statement is entered.

```
SUB A
TRG
SCAN ES00-ES47   (where E = extender number, S = slot number)
SUBEND
```

The subroutine will scan all channels on the FET multiplexer. Do not reset or cycle power to the HP 3852A or the subroutine will be erased from memory. The front panel CLEAR key may be used without disturbing the subroutine.

10-46 Opening Time Test

This test checks the time it takes for the FET to open after receiving an OPENING pulse from the FET multiplexer.

1. Repetitively call the entered subroutine 10000 times by executing:

```
CALL A,10000
```

This statement will call the subroutine 10000 times.

2. Observe the waveform displayed on the Channel B trace and make sure all 48 channels are present. It may also be necessary to adjust the TRIGGER LEVEL and TRIGGER HOLD controls, and to select the negative trigger pulse position on the scope to synchronize the signal on the scope.

3. Rotate the DELAY SWEEP dial to the minimum position. Select the DELAYED sweep mode on the scope. Slowly rotate the DELAY SWEEP dial clockwise while observing the displayed waveforms. The Channel B waveform is the OPENING pulse. The Channel A waveform is the +5V supply as switched by the relays. As the DELAY SWEEP dial is rotated, each channel switch and the associated OPENING pulse will come into view. The FET opening time is the time from the falling edge of the OPENING pulse to the rising edge of the Channel A waveform. This time must be less than 1.2 μseconds. The opening time is illustrated in Figure 10-28.

Continue rotating the DELAY Sweep dial until all 48 FET channels have been checked. A failing channel indicates a failing FET switch.

To stop the test at any time, press the front panel CLEAR key. The test time may be extended by by increasing the number of times the subroutine is called, as specified in step 1.

The waveform will exhibit a small amount of jitter due to the overhead requirements of the HP 3852A operating system.

10-47 Closing Time Test

This test checks the time it takes for the FET to close after receiving a CLOSING pulse from the FET multiplexer.

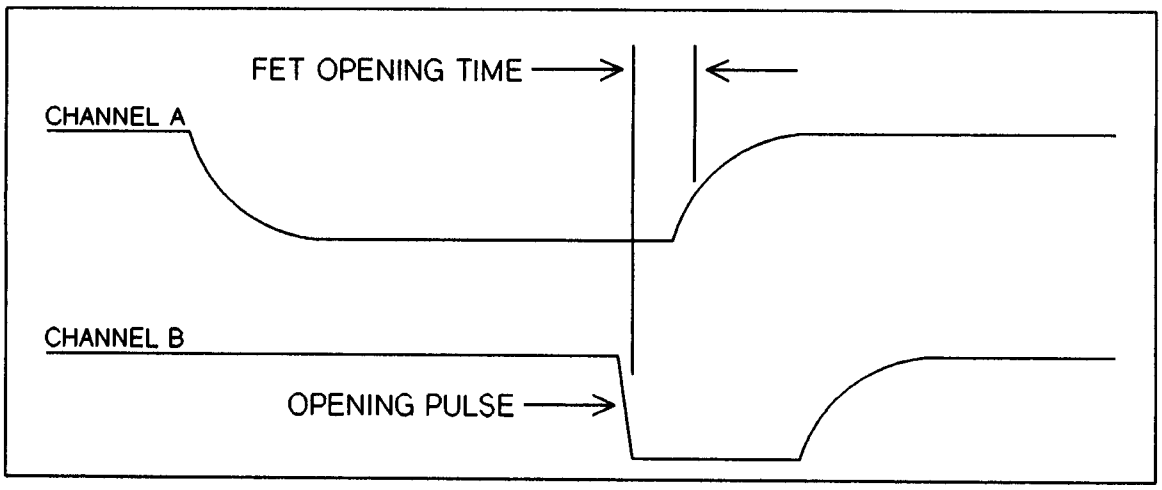


Figure 10-28 HP 44712A Opening Time

1. Move the channel B oscilloscope probe to the CLOSING connection on the service module. The Closing Time test set-up is shown in Figure 10-29.

2. Repetitively call the entered subroutine by executing:

CALL A,10000

3. Rotate the DELAY SWEEP dial on the oscilloscope to the minimum position. Slowly rotate the dial clockwise until the first closing is displayed. The Channel B trace is the closing pulse output from the multiplexer. The Channel A waveform is the +5V supply, as switched by the FET channel switches. As the DELAY SWEEP dial is rotated, each channel switch and the associated CLOSING pulse will come into view. The FET closing time is the time from the falling edge of the CLOSING pulse to the falling edge of the Channel A waveform. This time must be less than 2.25 µseconds. The closing time is illustrated in Figure 10-30.

Continue rotating the DELAY Sweep dial until all 48 FET channels have been checked. A failing channel indicates a failing FET switch.

To stop the test at any time, press the front panel CLEAR key. The test time may be extended by by increasing the number of times the subroutine is called, as specified in step 2.

The waveform will exhibit a small amount of jitter due to the overhead requirements of the HP 3852A operating system.

10-48 Leakage/Bias Current Test

The leakage current test checks the FET switches for excessive leakage/bias current. Leakage/bias current is sourced by the multiplexer from HIGH or LOW to chassis ground.

1. OPEN CHANNELS LEAKAGE/BIAS CURRENT TEST. This test checks the leakage current with all channels open. A simplified schematic of the setup is shown in Figure 10-31 and the test setup is shown in Figure 10-32.

2. Perform the Set-Up procedure in Section 10-40.

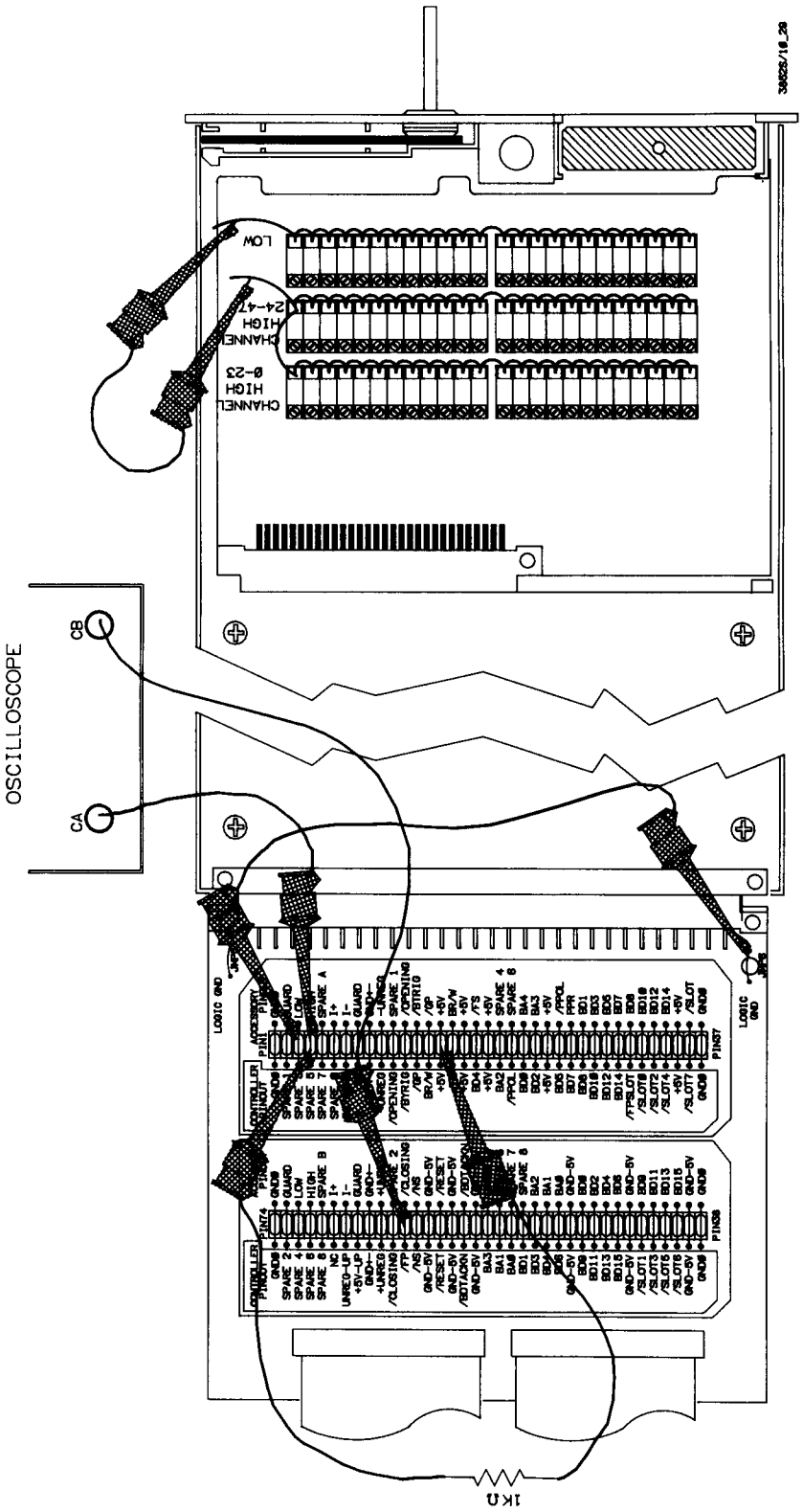


Figure 10-29 HP 44712A Closing Time Set-Up

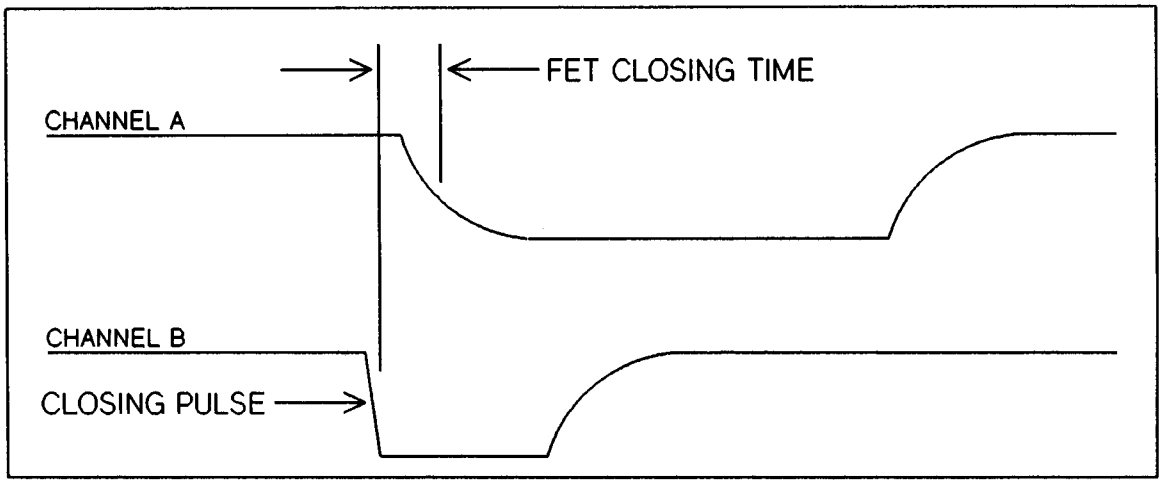


Figure 10-30 HP 44712A Closing Time

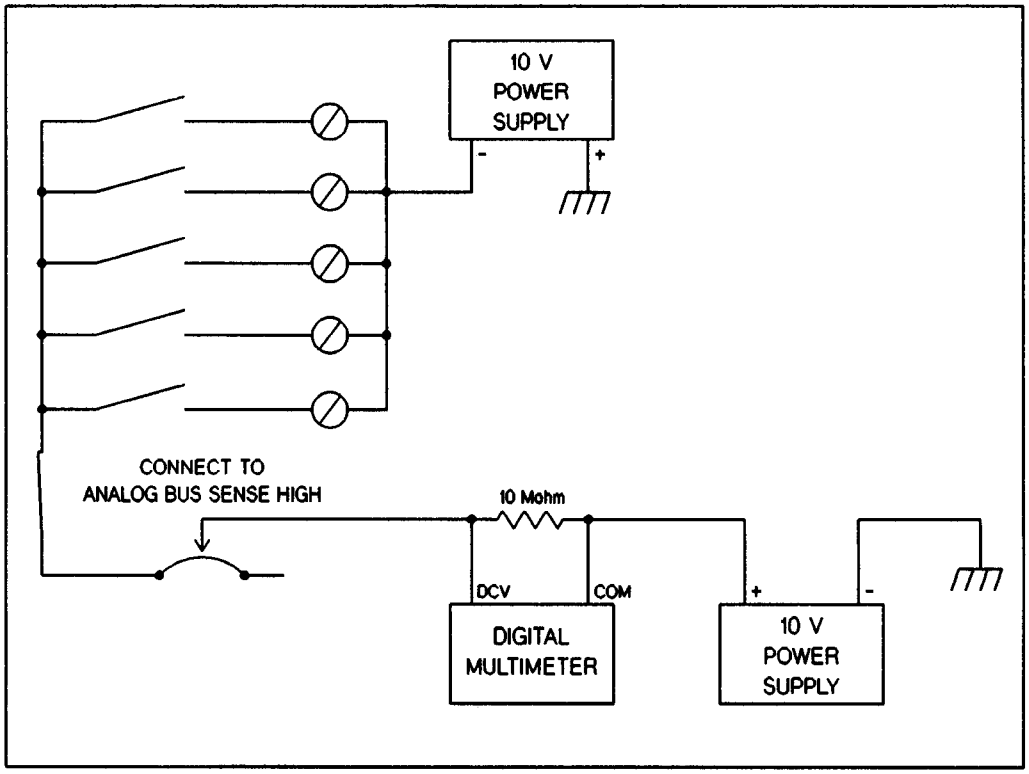


Figure 10-31 Open Channel Leakage Test

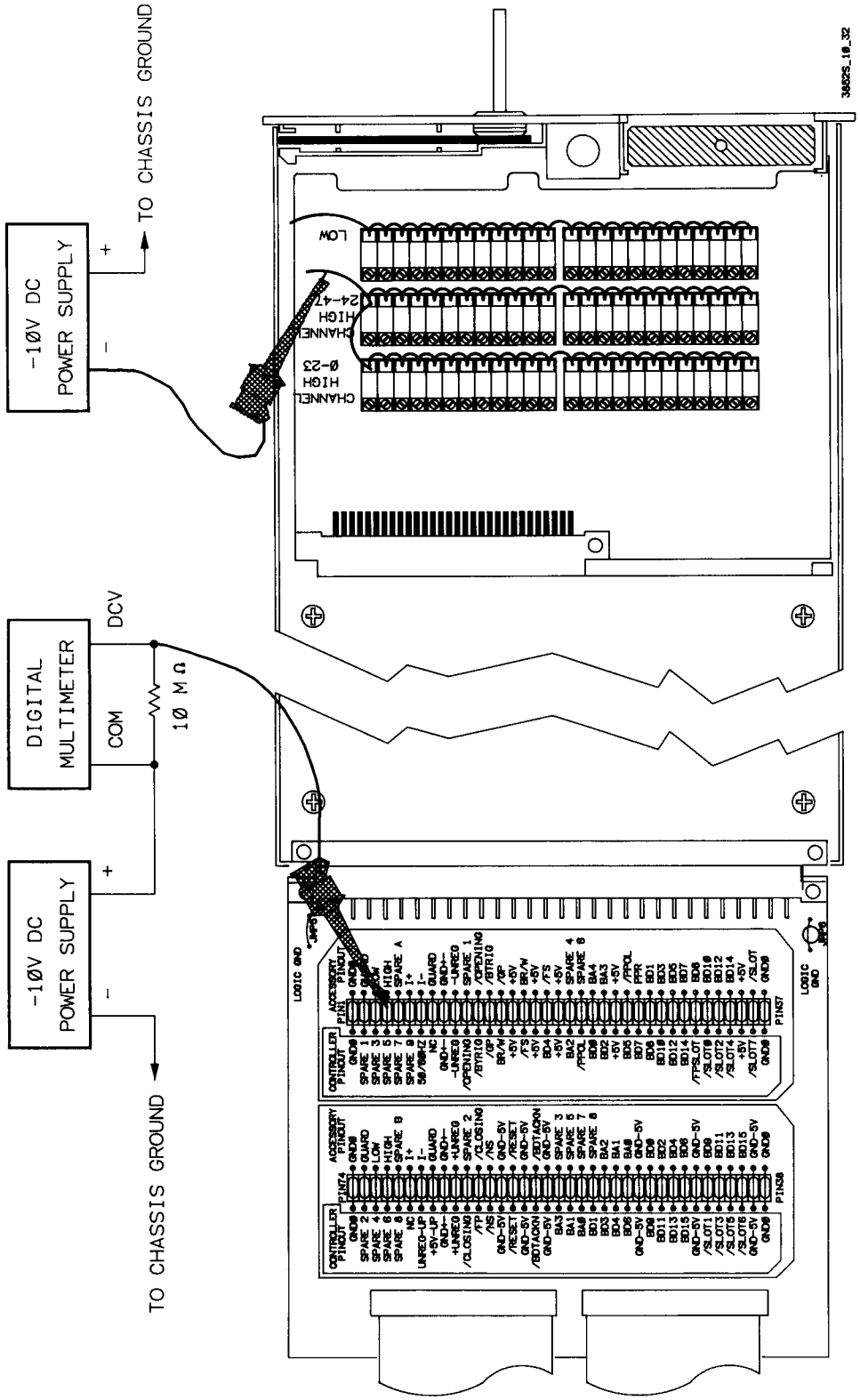


Figure 10-32 HP 44712A Open Channel Test Set-Up

3. Set the negative power supply output to 10 Vdc and connect the negative lead to the shorted HIGH lines on the test fixture. Connect the negative power supply common lead to the chassis.

NOTE

Connections to chassis ground can be accomplished by connecting to any sheet metal part. Chassis ground is also available at a connector on the rear panel of the HP 3852A power supply.

4. Set the positive power supply output to 10 Vdc and connect the positive lead to the multimeter common. Connect the positive power supply common to the chassis.

5. Connect the 10 Mohm resistor (**R1**) across the multimeter input terminals. Connect the multimeter DCV input terminal to the analog bus sense HIGH connection on the service module.

6. Open all switches on the multiplexer by executing:

RESET ES00 (where E = extender number, S = slot number)

7. Close the isolation relay and tree switches by executing:

CLOSE ES90,ES94 (where E = extender number, S = slot number)

8. Observe the reading on the multimeter. This reading is referred to as **V1** in the following steps.

9. Calculate the leakage current (**I**) from the formula:

$$I = \frac{V1}{R1}$$

The calculated open channel leakage current for the HIGH lines should be less than 2 nA for a room temperature between 0° and 28° C (for temperatures in the range of 0° to 55° C the leakage current should be less than 11 nA).

10. CLOSED CHANNEL LEAKAGE/BIAS CURRENT TEST. This test checks each channel HIGH lines for leakage current when a channel is closed. A simplified schematic of the setup is shown in Figure 10-31 and the test setup is shown in Figure 10-32.

11. Remove the negative power supply from the shorted HIGH lines on the test fixure.

12. Connect the shorted HIGH lines on the test fixure to the analog bus sense HIGH connection on the service module.

13. Connect the +10 V power supply common to chassis ground. Connect the power supply positive lead to the common lead of the multimeter.

14. Connect the 10 Mohm resistor across the multimeter input terminals. Connect the multimeter DCV input terminal to the shorted HIGH lines on the test fixture.

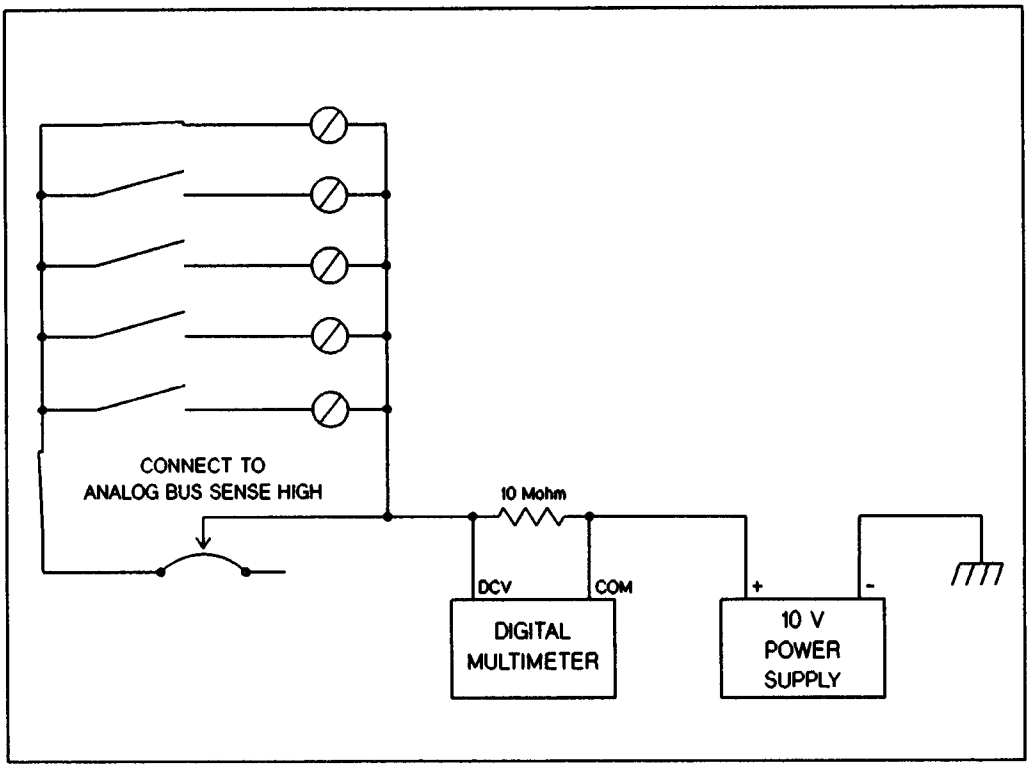


Figure 10-33 Closed Channel Leakage Test

15. Close the isolation relay by executing:

    CLOSE ES90 (where E = mainframe number, S = slot number)

16. Close the first channel in Bank A and the tree switches by executing:

    CLOSE ES94,ES00 (where E = mainframe number, S = slot number)

17. Observe the voltage reading on the multimeter. This voltage is referred to as **V1** in the following step.

18. Calculate the leakage current (I) from the formula:

$$I = \frac{V1}{R1}$$

The leakage current should be less than 5.0 nA for room temperatures in the range of 0° to 28° C (leakage current should be less than 15 nA for a temperature range of 28° to 55° C).

19. Repeat steps 16, 17, and 18 for channels 01 through 47. In step 16, the channel under test is specified in the second term of the CLOSE command (i.e., CLOSE ES94,ES01 for channel 01).

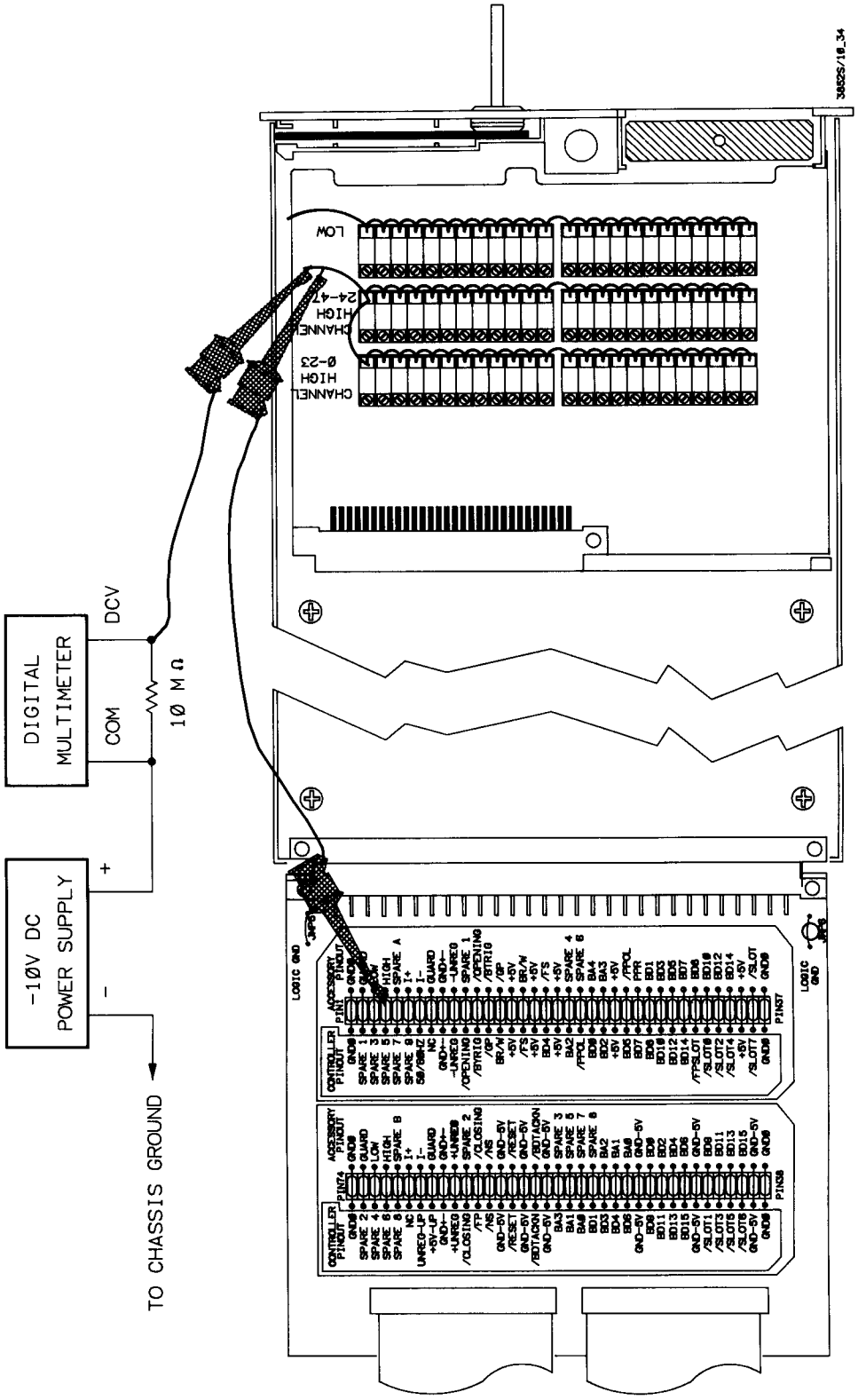


Figure 10-34 HP 44712A Closed Channel Test Set-Up

10-49 REPLACEABLE PARTS

Figure 10-35 shows the mechanical breakdown of the HP 44711A, HP 44712A and HP 44713A. The figure also provides assembly and disassembly information. The parts shown in Figure 10-35 are keyed to the parts lists in Table 10-9.

To order a part listed in Table 10-9, quote the Hewlett-Packard part number, the quantity desired, the HP system description, and the check digit (abbreviated CD in Table 10-9). Address the order to the nearest Hewlett-Packard Sales Office. Hewlett-Packard Sales Offices are listed geographically at the back of this manual.

CAUTION

The component module printed circuit board for the FET multiplexers is a static sensitive device. Refer to Chapter 5 for additional information about handling static sensitive printed circuit boards.

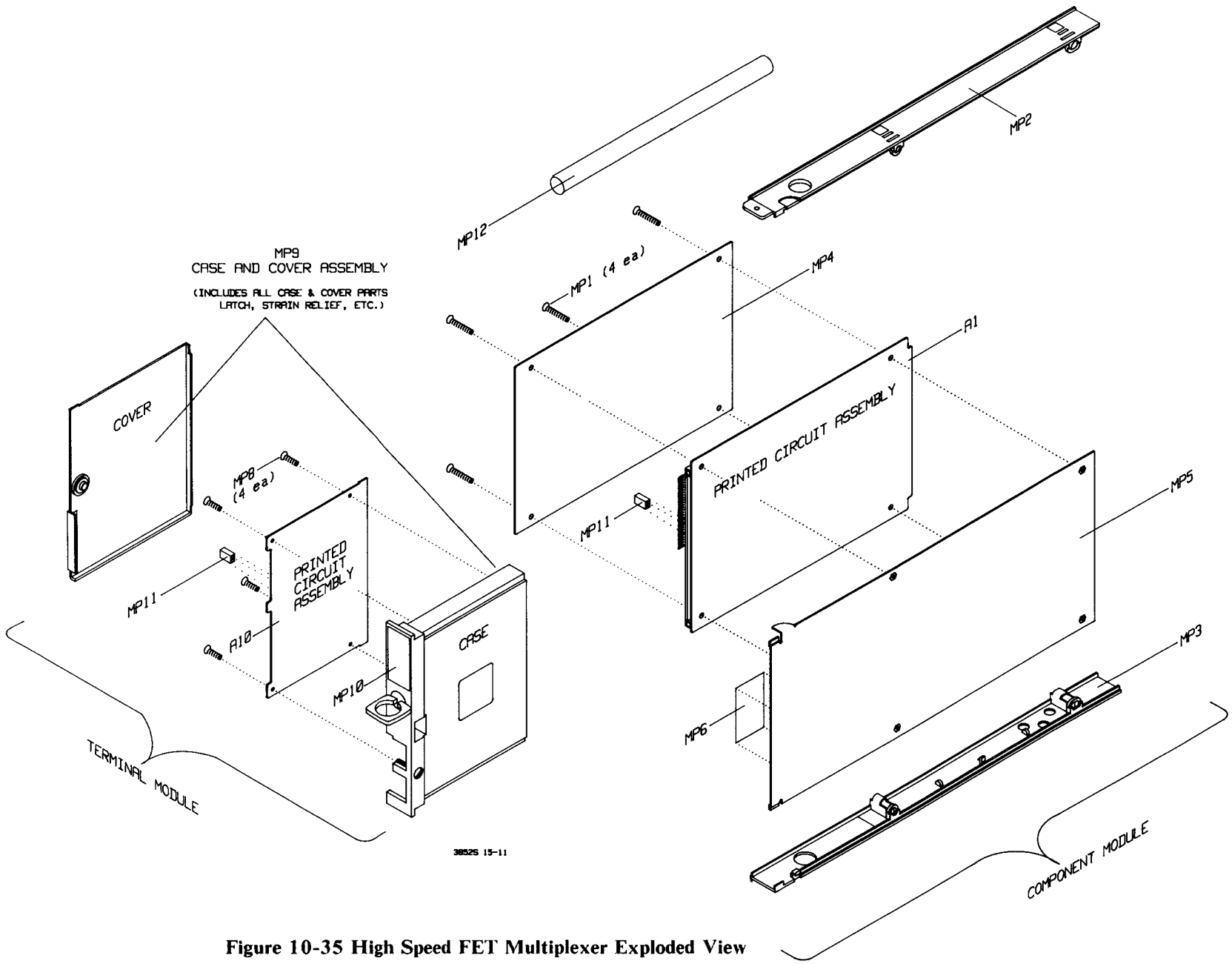


Figure 10-35 High Speed FET Multiplexer Exploded View

Table 10-9a HP 44711A 24 Channel High Speed FET Multiplexer

REF DESIG	DESCRIPTION	QTY	HP PART NUMBER	C D	HP FACTORY REFERENCE
44711A	Module; 24/48ch HS FET mux component	1	44711-66201	9	MOD-24/48CH FMUX
A1	PCA; 24/48 chan HS FET mux component	1	44711-66501	2	PCA-24/48CH FMUX
A10	PCA; 24 channel mux terminal	1	44711-66510	3	PCA-24CH GP TERM
MP1	Screw; cover	4	0515-1322	4	SCR-FH M3.0X30LK
MP2	Guide rail; top (molded)	1	03852-41201	1	MLD-RAIL,TOP
MP3	Guide rail; bottom (molded)	1	03852-41202	2	MLD-RAIL,BOTTOM
MP4	Cover; left (alum) w/ribbon-c access	1	44711-04101	8	0601 COV LEFT
MP5	Cover; right (alum) w/ribbn-c access	1	44711-04102	9	0601 COV RIGHT
MP6	Label; 44711/44712/44713 compont mod	1	44711-84320	1	LBL-I/O OPTIONS
MP7	Label; "STOP" internal cable warning	1	44711-84321	2	LBL-CAUTION-STOP
MP8	Screw; A10 PCA	4	0515-0886	3	SCR-PH M3.0X6 LK
MP9	Term box; case,cover,latch & str rlf	1	03852-84411	5	ASSY-TERM-SM OPN
MP10	Label; rear panel of term mod 44711A	1	44711-84325	6	LBL-ID,TERM ASSY

Completely assembled HP 44711A terminal modules can be ordered from your local HP Office by ordering Number 44711AT.

"447xx-662xx" and "447xx-692xx" part numbers are replacement components only and do not include a terminal module.

Restored Assemblies/Modules

The following restored assemblies/modules are available through the HP Exchange Program at a discount. For details see Section 1-19.

REF DESIG	DESCRIPTION	QTY	HP PART NUMBER	C D	HP FACTORY REFERENCE
44711A	Module; 24/48ch HS FET mux component		44711-69201	5	RBLT-44711-66201

44711B 11 (for use w/44704A) 44711-69202 RBLT-44711-66202

Table 10-9b HP 44712A 48 Channel High Speed Single Ended FET Multiplexer

REF DESIG	DESCRIPTION	QTY	HP PART NUMBER	C D	HP FACTORY REFERENCE
44712A	Module; 24/48ch HS FET mux component	1	44711-66201	9	MOD-24/48CH FMUX
A1	PCA; 24/48 chan HS FET mux component	1	44711-66501	2	PCA-24/48CH FMUX
A10	PCA; 48 chan single-end mux terminal	1	44712-66510	4	PCA-48CH,SE TERM
MP1	Screw; cover	4	0515-1322	4	SCR-FH M3.0X30LK
MP2	Guide rail; top (molded)	1	03852-41201	1	MLD-RAIL,TOP
MP3	Guide rail; bottom (molded)	1	03852-41202	2	MLD-RAIL,BOTTOM
MP4	Cover; left (alum) w/ribbon-c access	1	44711-04101	8	0601 COV LEFT
MP5	Cover; right (alum) w/ribbn-c access	1	44711-04102	9	0601 COV RIGHT
MP6	Label; 44711/44712/44713 compont mod	1	44711-84320	1	LBL-I/O OPTIONS
MP7	Label; "STOP" internal cable warning	1	44711-84321	2	LBL-CAUTION-STOP
MP8	Screw; A10 PCA	4	0515-0886	3	SCR-PH M3.0X6 LK
MP9	Term box; case,cover,latch & str rlf	1	03852-84411	5	ASSY-TERM-SM OPN
MP10	Label; rear panel of term mod 44712A	1	44712-84325	7	LBL-ID,TERM ASSY

Completely assembled HP 44712A terminal modules can be ordered from your local HP Office by ordering Number 44712AT.

"447xx-662xx" and "447xx-692xx" part numbers are replacement components only and do not include a terminal module.

Restored Assemblies/Modules

The following restored assemblies/modules are available through the HP Exchange Program at a discount. For details see Section 1-19.

REF DESIG	DESCRIPTION	QTY	HP PART NUMBER	C D	HP FACTORY REFERENCE
44712A	Module; 24/48ch HS FET mux component		44711-69201	5	RBLT-44711-66201

Table 10-9c HP 44713A 24 Channel High Speed FET Mux with Thermocouple Compensation

REF DESIG	DESCRIPTION	QTY	HP PART NUMBER	C D	HP FACTORY REFERENCE
44713A	Module; 24/48ch HS FET mux component	1	44711-66201	9	MOD-24/48CH FMUX
A1	PCA; 24/48 chan HS FET mux component	1	44711-66501	2	PCA-24/48CH FMUX
A10	PCA; 24 chan mux term w/TC reference	1	44713-66510	5	PCA-24CH TC COMP
MP1	Screw; cover	4	0515-1322	4	SCR-FH M3.0X30LK
MP2	Guide rail; top (molded)	1	03852-41201	1	MLD-RAIL,TOP
MP3	Guide rail; bottom (molded)	1	03852-41202	2	MLD-RAIL,BOTTOM
MP4	Cover; left (alum) w/ribbon-c access	1	44711-04101	8	0601 COV LEFT
MP5	Cover; right (alum) w/ribbn-c access	1	44711-04102	9	0601 COV RIGHT
MP6	Label; 44711/44712/44713 compont mod	1	44711-84320	1	LBL-I/O OPTIONS
MP7	Label; "STOP" internal cable warning	1	44711-84321	2	LBL-CAUTION-STOP
MP8	Screw; A10 PCA	4	0515-0886	3	SCR-PH M3.0X6 LK
MP9	Term box; case,cover,latch & str rlf	1	03852-84411	5	ASSY-TERM-SM OPN
MP10	Label; rear panel of term mod 44713A	1	44713-84325	8	LBL-ID,TERM ASSY

Completely assembled HP 44713A terminal modules can be ordered from your local HP Office by ordering Number 44713AT.

"447xx-662xx" and "447xx-692xx" part numbers are replacement components only and do not include a terminal module.

Restored Assemblies/Modules

The following restored assemblies/modules are available through the HP Exchange Program at a discount. For details see Section 1-19.

REF DESIG	DESCRIPTION	QTY	HP PART NUMBER	C D	HP FACTORY REFERENCE
44713A	Module; 24/48ch HS FET mux component		44711-69201	5	RBLT-44711-66201